hynix

1GB e-NAND
H26M11001BAR

Document Title
e-NAND

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	Jun. 24. 2009	
1.0	Released 1.0 spec. for e-NAND	Sep. 29. 2009	

1. Introduction

1.1 General Description

The Hynix e-NAND Module is a very small, flash storage device, designed specifically for storage applications that put a premium on small form factor, low power and low cost. Flash is the ideal storage medium for portable, battery-powered devices. It features lowpower consumption and is non-volatile, requiring no power to maintain the stored data. It also has a wide operating range for temperature, shock and vibration.e-NAND is well-suited to meet the needs of small, low power, electronic devices. e-NAND is expected to be used in a wide variety of portable devices like mobile phones, PMP, Smart phones, PDA, Media Players and etc. To support this wide range of applications, the e-NAND is offered with an MMC Interface, fully compatible with MMC Interface, and provides a 8-bit data bus for maximum performance. These interfaces allow for easy integration into any design, regardless of which type of microprocessor is used. All device and interface configuration data (such as maximum frequency and module identification) are stored on the device. In addition to the mass-storage-specific flash memory chip, the e-NAND module includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management, wear leveling, and clock control. Figure 1-1 is a block diagram of the Hynix e-NAND module with MMC Interface.

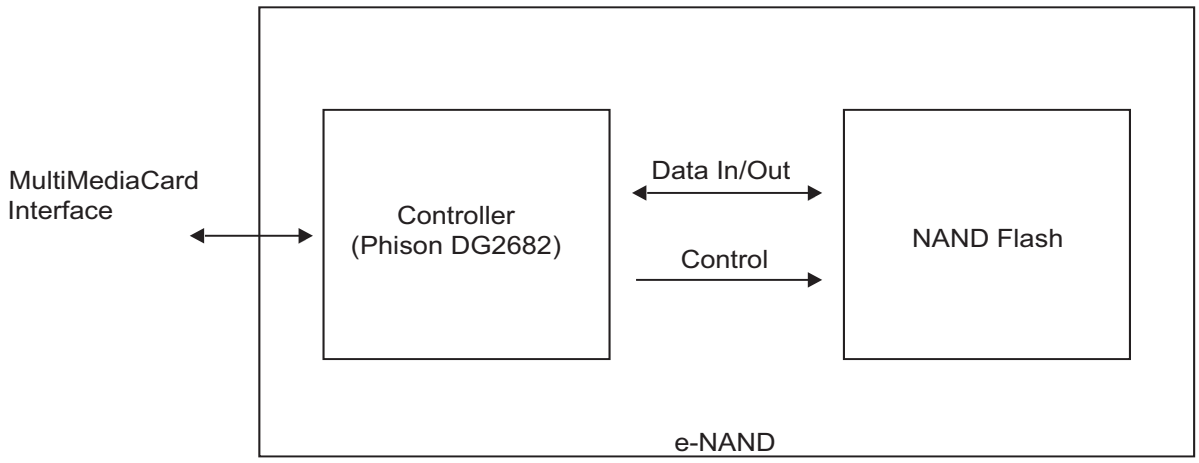


Figure 1-1 : e-NAND Block Diagram

1.2 System Features

- JEDEC JESD84 V4.3 compatible
- Backward compatible with earlier JESD84
- Maximum data rate with up to 52MB/sec interface speed (using 8 parallel data lines)
- Voltage Range :

	Voltage
Communication	1.7 - 1.95 or 2.7 - 3.6
Memory Access	2.7 - 3.6

- e-NAND supported clock frequencies 0~20MHz, 0~26MHz, 0~52MHz
- e-NAND support for three different data bus width modes: 1bit(default), 4bit and 8 bit
- Correction of memory field errors
- Simple erase mechanism
- Password Protection of e-NAND

1.2.1 Product List

PART NUMBER	DENSITY	JEDEC JESD84 SPEC	PACKAGE
H26M11001BAR	1GB	V4.3	169-FBGA (12x16x1.3)

1.3 Flash Independent Technology

The 512 byte sector size of the Hynix e-NAND is the same as that in an IDE magnetic disk drive.
To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the e-NAND. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Because the e-NAND uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves.

1.4 Defect and Error Management

The Hynix e-NAND contain a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. For instance, disk drives do not typically perform a read after write to confirm the data is written correctly because of the performance penalty that would be incurred. e-NAND do a read after write under margin conditions to verify that the data is written correctly (except in the case of a Write without Erase Command). In the rare case that a bit is found to be defective. e-NAND will even replace the entire sector with a spare sector. This is completely transparent to the host and does not consume any user data space. The e-NAND soft error rate specification is much better than the magnetic disk drive specification. In the extremely rare case a read error does occur, e-NAND have innovative algorithms to recover the data. This is similar to using retries on a disk drive but is much more sophisticated. The last line of defense is to employ powerful ECC to correct the data. If ECC is used to recover data, defective bits are replaced with spare bits to ensure they do not cause any future problems. These defect and error management systems coupled with the solid-state construction give e-NAND unparalleled reliability.

1.5 Sleep Mode (CMD5)

A card may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. In this state the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. The timeout for state transitions between Standby state and Sleep state is defined in the EXT_CSD register S_A_timeout. The maximum current consumptions during the Sleep state are defined in the EXT_CSD registers S_A_VCC and S_A_VCCQ.
Sleep command: The bit 15 as set to 1 in SLEEP/AWAKE (CMD5) argument.
Awake command: The bit 15 as set to 0 in SLEEP/AWAKE (CMD5) argument.
The Sleep command is used to initiate the state transition from Standby state to Sleep state. The memory device indicates the transition phase busy by pulling down the DAT0 line. No further commands should be sent during the busy. The Sleep state is reached when the memory device stops pulling down the DAT0 line.
The Awake command is used to initiate the transition from Sleep state to Standby state. The memory device indicates the transition phase busy by pulling down the DAT0 line. No further commands should be sent during the busy. The Standby state is reached when the memory device stops pulling down the DAT0 line.
During the Sleep state the Vcc power supply may be switched off. This is to enable even further system power consumption saving. The Vcc supply is allowed to be switched off only after the Sleep state has been reached (the memory device has stopped to pull down the DAT0 line). The Vcc supply have to be ramped back up at least to the min operating voltage level before the state transition from Sleep state to Standby state is allowed to be initiated (Awake command).

1.6 MMC Mode

1.6.1 e-NAND Standard Compliance

The Hynix e-NAND is fully compliant with JEDEC JESD84 V4.3 series of specifications.

1.6.2 Negotiating Operation Conditions

The e-NAND supports the operation condition verification sequence defined in the JEDEC JESD84 V4.3 series of specifications. The e-NAND host should define an operating voltage range that is not supported by the e-NAND. It will put itself in an inactive state and ignore any bus communication. The only way to get the e-NAND out of the inactive state is by powering it down and up again. In addtion the host can explicitly send the e-NAND to the inactive state by using the GO_INACTIVE _STATE command.

1.6.3 Card Status

e-NAND status is stored in a 32 bit status register which is sent as the data field in the card respond to host commands. Status register provides information about the card's current state and completion codes for the last host command. The card status can be explicityly read(polled) with the SEND_STATUS command.

1.6.4 Memory Array Partitioning

The basic unit of data transfer to/from the e-NAND is one byte. All data transfer operations which require a block size always define block lenghs as integer multiples of bytes. Some special functions need other partition granularity.

For block oriented commands, the following definition is used:

- Block: is the unit which is related to the block oriented read and write commands. Its size is the number of bytes which will be transferred when one block command is sent by host. The size of a block is either programable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.

For R/W cards, special erase and write protect commands are defined:

- The granularity of the erasable units is the Erase Group: The smallest number of consecutive write blocks which can be addressed for erase. The size of the Erase Group is card specific and stored in the CSD.
- The granularity of the Write Protected units is the WP-Group: The minimal unit which may be individually write protected. Its size is defined in units of erase groups. The size of a WP-Group is card specific and stored in the CSD.

1.6.5 Read and Write Operations

The e-NAND supports two read/write modes.

Single Block Mode

In this mode the host read or write one data block in a pre-specified length block transmission is protected with 16bit CRC which is generated by the sending unit and checked by the receiveing unit. Misalignment is not allowed. Every data block must be contained in a single memroy sector. The block length for write opertaion must be identical to the sector size and the start address aligned to a sector boundary.

Multiple Block Mode

This mode is similar to the single block mode, but the host can read/write multiple data blocks (all have the same length) which will be stored or retrived from contiguous memory addresses starting at the address specified in the command. The operation is terminated with a stop transmission command. Misalignment and block length restrictions apply to multiple blocks as well and are identical to the single block read/write operations. Multiple block read with pre-defined block is supported.

1.6.6 Data Protection in the e-NAND

Every sector is protected with an Error Correction Code (ECC). The ECC is generated (in the e-NAND) when the sectors are written and validated when the data is read. If defects are found, the data is corrected prior to transmission to the host. The e-NAND can be considered error free and no additional data protection is needed. However, if an application uses additional, external, ECC protection, the data oragnization is defined in the user writeable section of the CSD register.

1.6.7 Erase

The smallest erasable unit in the e-NAND is a erase group. In order to speed up the erase procedure, multiple erase groups can be erased in the same time. The erase operation is divided into two stages.

Tagging - Selecting the Sectors for Erasing

To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all erase groups within this range will be selected for erase.

Erasing - Starting the Erase Process

Tagging can address erase groups. An arbitrary selection of erase groups may be erased at one time. Tagging and erasing must follow a strict command sequence (refer to the e-NAND standard sepcification for datails).

1.6.8 Write Protection

Two-card level write-protection options are available: permanent and temporary. Both can be set using the PROGRAM_CSD command (refer to CSD Programming, Section 4.2.8). The permanent write protect bit, once set, cannot be clearded. This feature is implemented in the e-NAND controller firmware and not with a physical OTP cell.

1.6.9 Copy Bit

The content of an e-NAND can be marked as an original or a copy using the copy bit in the CSD register. Once the Copy bit is set (maked as original) it cannot be cleared. The Copy bit of the e-NAND is programmed (during test and formatting on the manufacturing floor) as a copy. The e-NAND can be purchased with the copy bit set (copy) or cleared, indicating the card is a master. The One Time Programmable (OTP) characteristic of the Copy bit is implemented in the e-NAND controller firmware and not with a physical OTP cell.

1.6.10 The CSD Register

All the configuration information of the e-NAND is stored in the CSD register.

The host can read the CSD register and alter the host controlled data bytes using the SEND_CSD and PROGRAM_CSD commands.

2. Product Specifications

2.1 Environmental Characteristics

Vddi for internal power stability

Parameter	Value	Unit
Operation Temperature	-25 to 85	℃
Storage Temperature	-40 to 85	℃

3. Interface Description

3.1 Physical Description

3.1.1 Pin Assignments

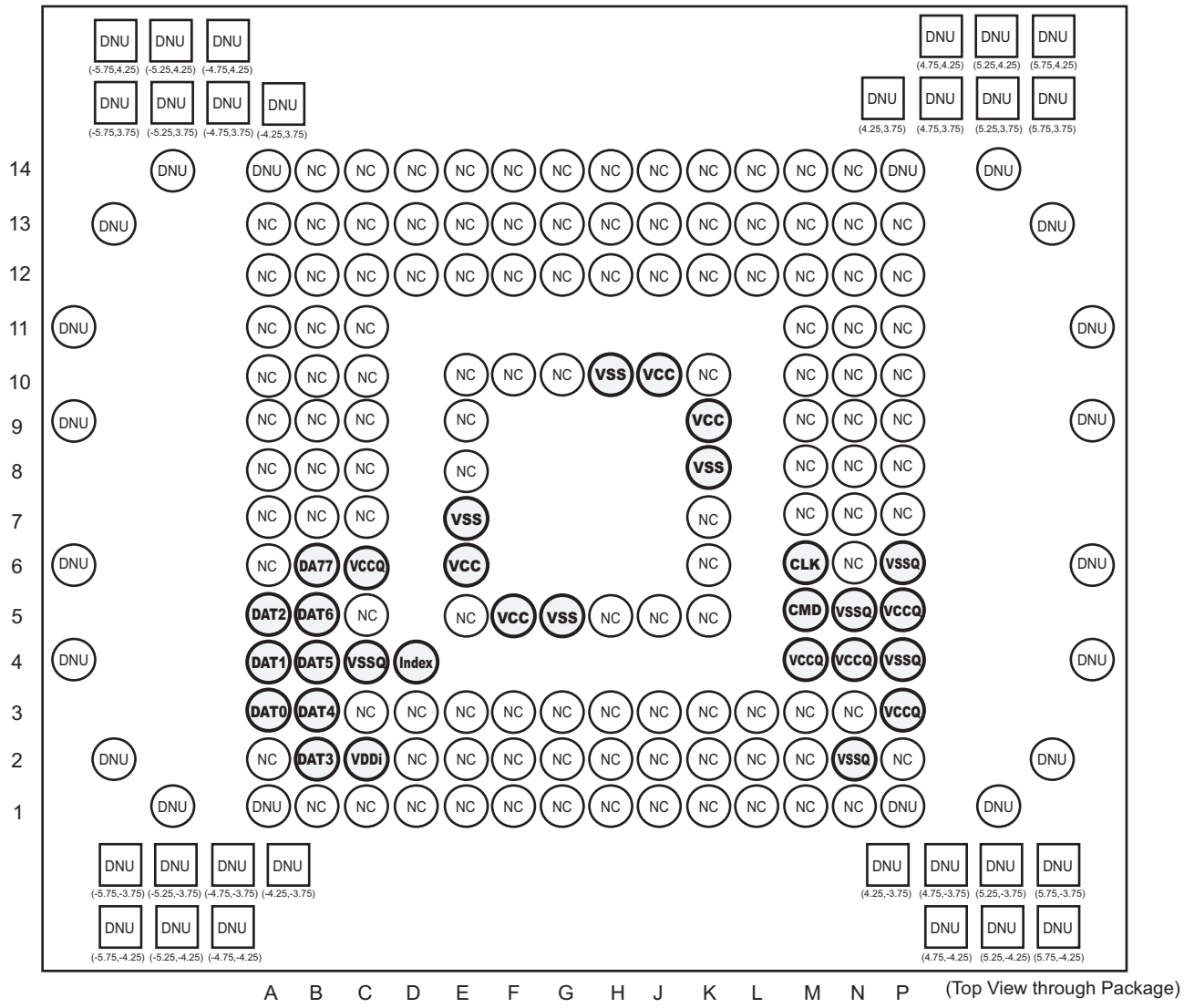


Figure 3-1 : e-NAND Pin Configuration

Pins	MMC Interface		
	Name	IO Type(1)	Description
M5	CMD	I/O/PP/OD	Command / Response
M6	CLK	I	Clock
E7, G5, H10, K8	Vss	S	Flash Memory Supply Voltage Ground
C4, N2, N5, P4, P6	Vssq	S	Core Supply Voltage Ground
C6, M4, N4, P3, P5	Vccq	S	Core Supply Voltage
E6, F5, J10, K9	Vcc	S	Flash Memory Supply Voltage
A3	DATA0	I/O/PP	Data
A4	DAT1	I/O/PP	Data
A5	DAT2	I/O/PP	Data
B2	DAT3	I/O/PP	Data
B3	DAT4	I/O/PP	Data
B4	DAT5	I/O/PP	Data
B5	DAT6	I/O/PP	Data
B6	DAT7	I/O/PP	Data
C2	VDDi	-	The capacitor (0.1μF) must be connected for internal power stability.
NC	Not Connected		
DNU	Do Not Use		

Table 3-1 : Pin Description

Note:
1. S: Power Supply; I: input; O: output; PP: push-pull; OD: open-drain;
2. The DAT0-DAT7 pins for read-only cards are output only

3.2 e-NAND Bus Topology

The e-NAND bus has ten communication lines:

- CMD: Command is a bidirectional signal. The host and e-NAND drivers are operating in two modes, open drain and push pull.
- DAT0-7: Data lines are bidirectional signals. Host and e-NAND drivers are operating in push pull mode
- CLK: Clock is a host to e-NAND signal. CLK operates in push pull mode
- Vccq: Vccq is the power supply line for Core signal
- Vcc: Vcc is the power supply line for Flash Memory
- Vddi: The capacitor (0.1μF min.) Must be connected to Vddi for internal power stability
- Vss, Vssq are two ground lines

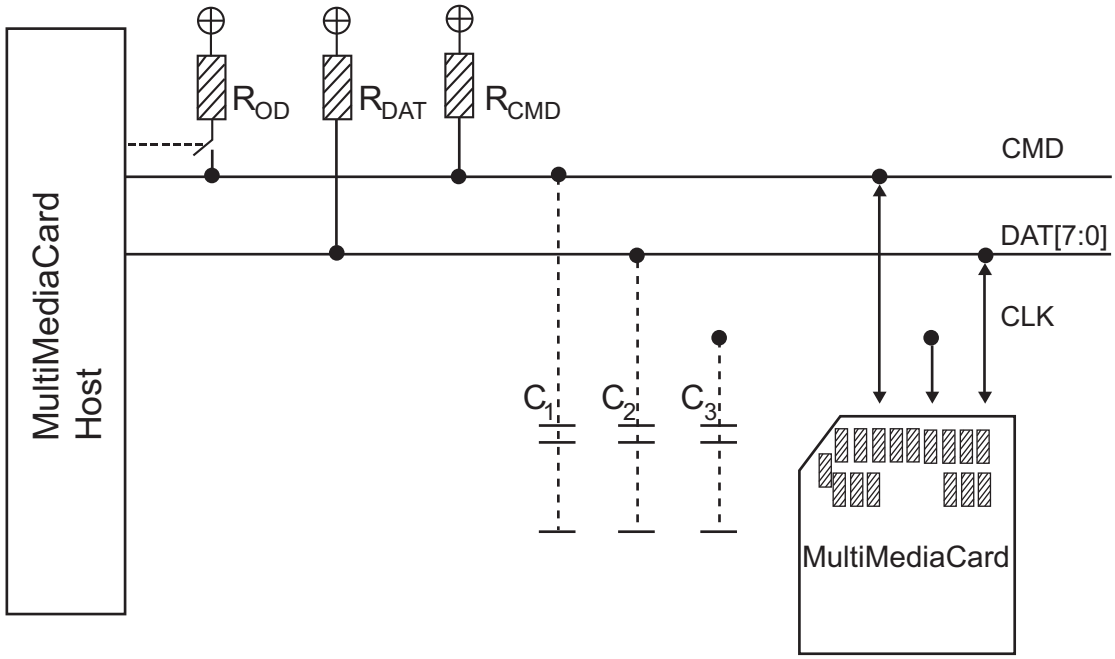


Figure 4-3 : Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating when no card is inserted or when all card drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used (the minimum value is defined in the Chapter). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in Table 3-4.

The host is recommended to connect capacitor to Vddi for e-NAND's internal power stability.

3.3.2 e-NAND power-up

The e-NAND bus power-up is handled locally in each device and in the bus master. Figure 3-4 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence.

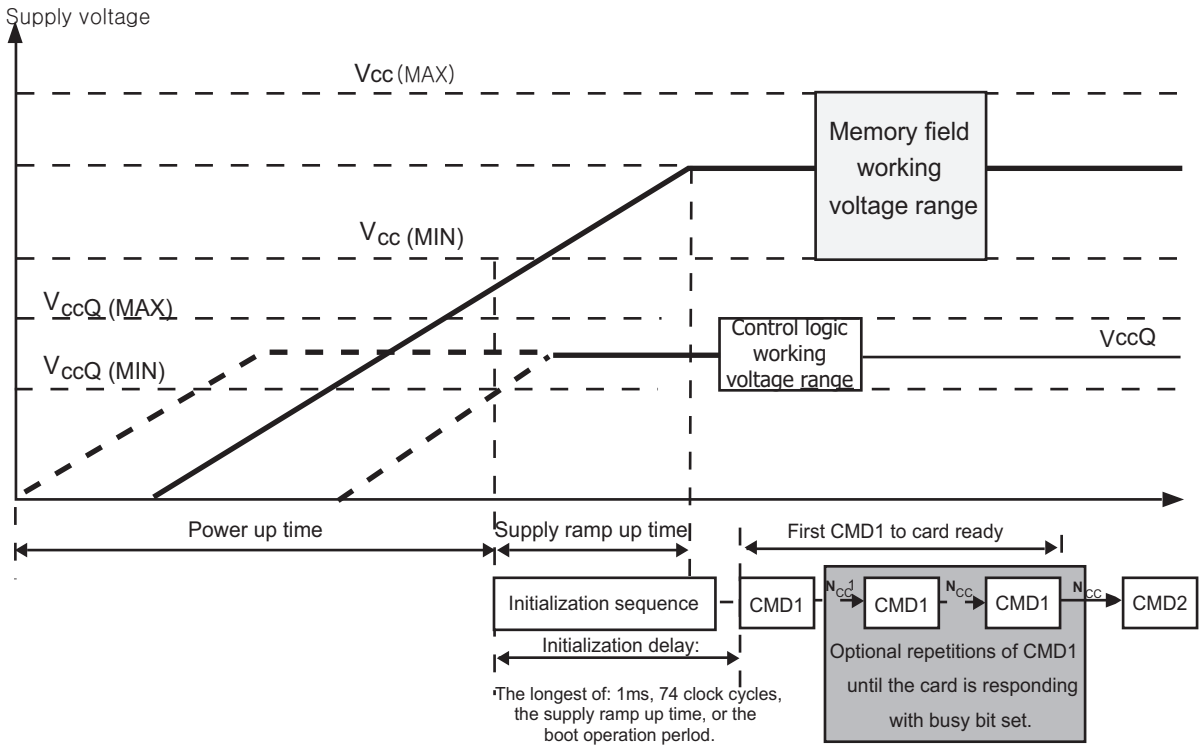


Figure 3-4 : e-NAND Power-up Diagram

3.3.3 e-NAND power-up guidelines

The e-NAND power-up must adhere to the following guidelines:

- When power-up is initiated, either VCC or VCCQ can be ramped up first, or both can be ramped up simultaneously.
- After power up, the e-NAND enters the pre-idle state.
- If the e-NAND does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, the e-NAND moves immediately to the idle state. While in the idle state, the e-NAND ignores all bus transactions until CMD1 is received. If the e-NAND supports only specification v4.2 or earlier versions, the device enters the idle state immediately following power-up.
- If the BOOT_PARTITION_ENABLE bit is set, the e-NAND moves to the pre-boot state, and the e-NAND waits for the boot-initiation sequence. Following the boot operation period, the e-NAND enters the idle state. During the pre-boot state, if the e-NAND receives any CMD-line transaction other than the boot initiation sequence (keeping CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA) and CMD1, the e-NAND moves to the Idle state. If the e-NAND receives the boot initiation sequence (keeping the CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA), the e-NAND begins boot operation. If boot acknowledge is enabled, the e-NAND shall send acknowledge pattern "010" to the host within the specified time. After boot operation is terminated, the e-NAND enters the idle state and shall be ready for CMD1 operation. If the e-NAND receives CMD1 in the pre-boot state, it begins responding to the command and moves to the card identification mode.
- While in the idle state, the e-NAND ignores all bus transactions until CMD1 is received.
- CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the device until it is out of its power-up sequence. In addition to the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.
- The bus master moves the device out of the idle state. Because the power-up time and the supply ramp up time depend on application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.
- After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.
- Every bus master must implement CMD1.

3.3.4 e-NAND power cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master with host must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave with the e-NAND enters sleep mode, the master with host can power-down VCC to reduce power consumption. It is necessary for the slave with e-NAND to be ramped up to VCC

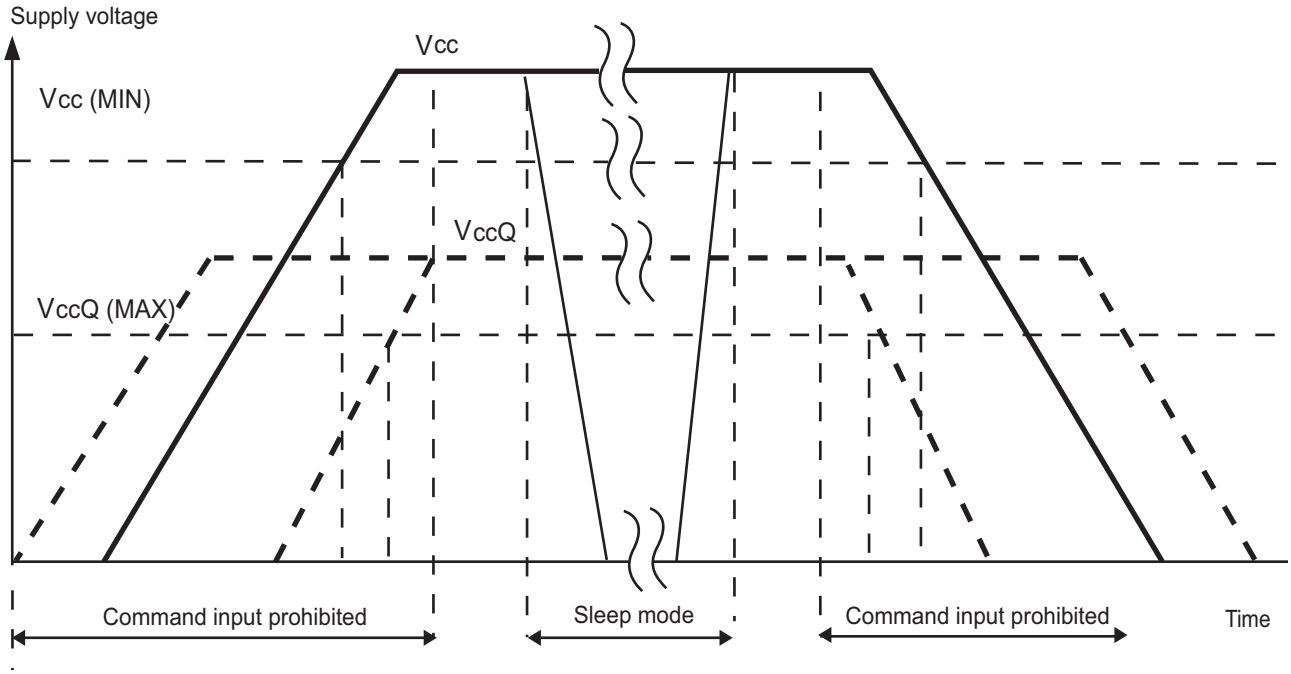


Figure 3-5: The e-NAND power cycle

3.3.5 Bus Operating Conditions

General

Parameter		Symbol	Min	Max.	Unit	Remark
Peak voltage on lines	BGA		-0.5	VccQ+0.5	V	
All Inputs						
Input Leakage Current(before initialization sequenceand/or the internal pull up resistors connected)			-100	100	μA	
Input Leakage Current(after initialization sequence and the internal pull up resistors disconnected)			-10	10	μA	
All Inputs						
Output Leakage CurrentCurrent (before initialization sequence)			-100	100	μA	
Output Leakage Current(after initialization sequence)			-10	10	μA	

Table 3-2 : Bus Operating Conditions

Power Supply Voltage - e-NAND

Parameter	Symbol	Min	Max.	Unit	Remark
Supply voltage (NAND)	Vcc	2.7	3.6	V	
Supply voltage (I/O)	Vccq	2.7	3.6	V	
		1.7	1.95	V	

Table 3-3 : Power Supply Voltage

3.3.6 Bus Signal Line Load

The total capacitance C_L of each line of the e-NAND bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance $C_{e\text{-}NAND}$ of the card connected to this line:

$C_L = C_{HOST} + C_{BUS} + C_{e\text{-}NAND}$

Requiring the sum of the host and bus capacitances not to exceed 20 pF:

Parameter	Symbol	Min	Typ	Max.	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	50		100	KOhm	to prevent bus floating
Bus signal line capacitance	C_L			30	pF	Single Card
e-NAND capacitance	C_{BGA}		7	12		
Maximum signal line inductance				16	nH	fPP <= 52 MHz

Table 3-4 : Host and Bus Capacities

3.3.7 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

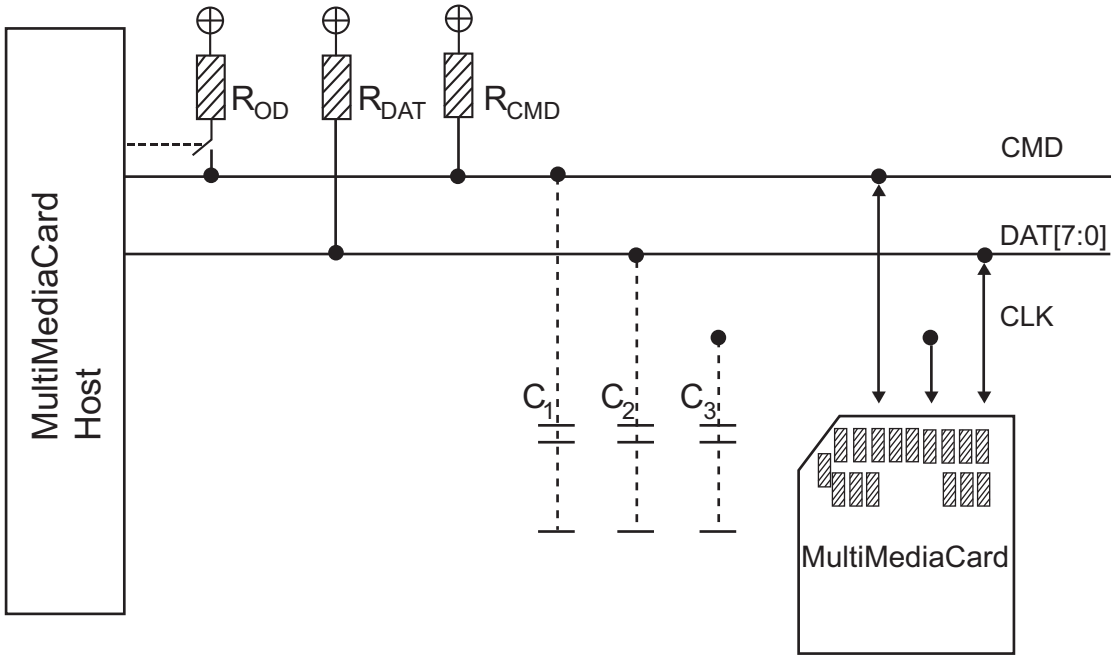


Figure 43: Bus Circuitry Diagram

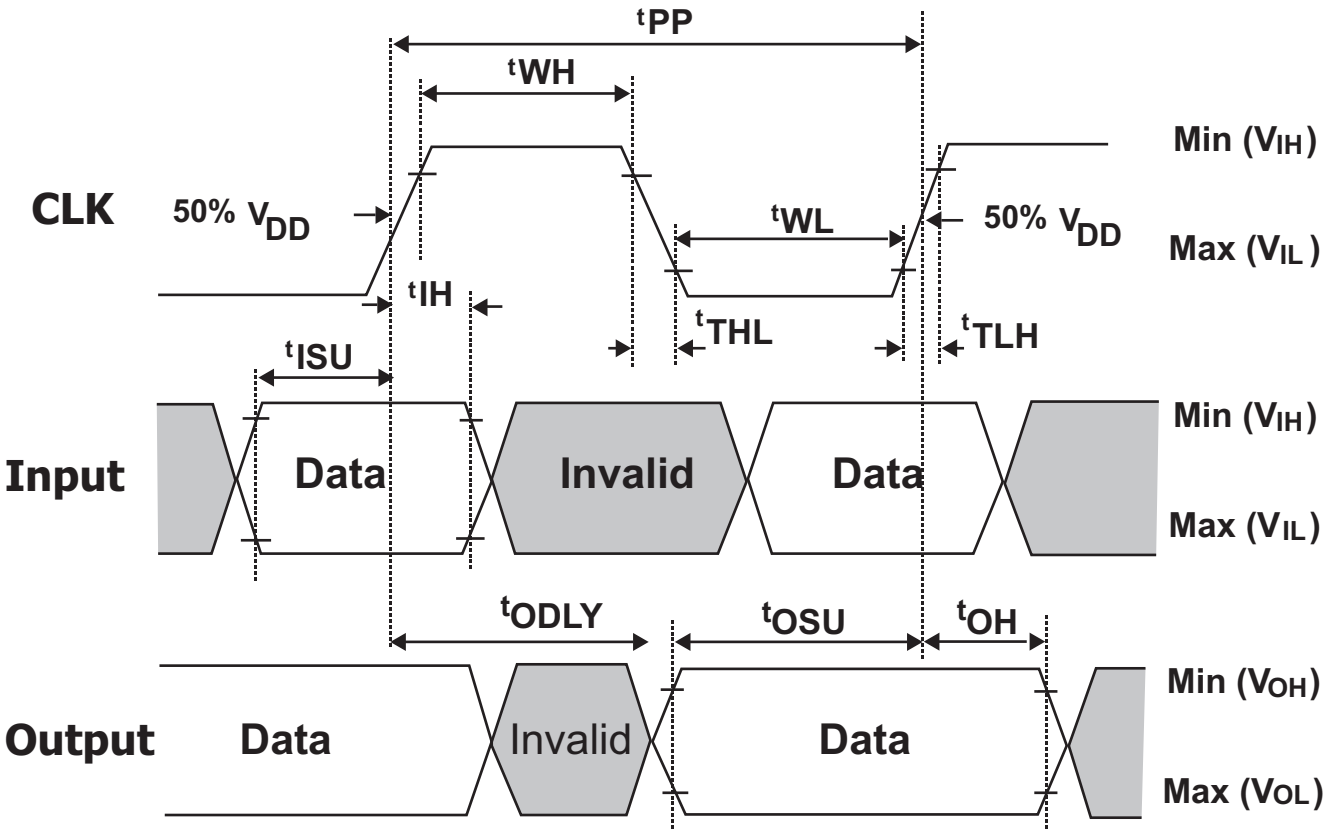
3.3.9 Push-Pull Mode Bus Signal Level - e-NAND

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any Vccq of the allowed voltage range:

Parameter	Symbol	Min		Max.		Unit	Conditions
		1.7 - 1.95V	2.7 - 3.6V	1.7 - 1.95V	2.7 - 3.6V		
Output HIGH voltage	V_{OH}	V_{ccq} - 0.2V	0.75*V_{ccq}			V	I_{OH}=-100 mA @V_{ccq} min
Output LOW voltage	V_{OL}			0.2V	0.125*V_{ccq}	V	I_{OL}=100 mA @V_{ccq} min
Input HIGH voltage	V_{IH}	0.7*V_{ccq}	0.625*V_{ccq}	V_{ccq} + 0.3	V_{ccq} + 0.3	V	
Input LOW voltage	V_{IL}	VSS-0.3	VSS-0.3	0.3*V_{ccq}	0.25*V_{ccq}	V	

Table 3-6 : Push-Pull Mode Bus Signal Level - Vccq

3.3.10 Bus & e-NAND Interface Timing



Data must always be sampled on the rising edge of the clock.

Figure 3-7 : Timing Diagram: Data Input/Output

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[a]					
Clock frequency Data Transfer Mode (PP)[b]	f_{PP}	0	52[c]	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock rise time[d]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	C_L <= 30 pF
Output hold time	t_{OH}	2.5		ns	C_L <= 30 pF
Signal rise time[e]	t_{rise}		3	ns	C_L <= 30 pF
Signal fall time	t_{fall}		3	ns	C_L <= 30 pF

a.All timing values are measured relative to 50% of voltage level
b.The e-NAND supports full frequency range from 0-26Mhz, or 0-52MHz
c.Card can operate as high-speed card interface timing at 26 MHz clock frequency.
d.CLK rise and fall times are measured by min (VIH) and max (VIL).
e.Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 3-6 : High Speed e-NAND Interface Timings

Parameter	Symbol	Min	Max.	Unit	Remark[a]
Clock CLK[b]					
Clock frequency Data Transfer Mode (PP)[c]	f_{PP}	0	26	MHz	CL <= 30 pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10		ns	CL <= 30 pF
Clock rise time[d]	t_{TLH}		10	ns	CL <= 30 pF
Clock fall time	t_{THL}		10	ns	CL <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	CL <= 30 pF
Input hold time	t_{IH}	3		ns	CL <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF

a.The card must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
b.All timing values are measured at 50% of voltage level.
c.For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.
d.CLK rise and fall times are measured by min (VIH) and max (VIL).

Table 3-7 : Backwards Compatible e-NAND Interface

3.4 e-NAND Registers

Within the e-NAND interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands. The OCR, CID and CSD registers carry the e-NAND/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both, e-NAND specific information and actual configuration parameters.

3.4.1 OCR Register

The 32-bit operation conditions register stores the Vccq voltage profile of the e-NAND. In addition, this register includes a status information bit. This status bit is set if the e-NAND power up procedure has been finished. The OCR register shall be implemented by e-NAND.

OCR bit	Vccq voltage window	e-NAND
[6:0]	Reserved	000 0000b
[7]	1.7 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	e-NAND power up status bit (busy)[a]	

a.This bit is set to LOW if the e-NAND has not finished the power up routine

The supported voltage range is coded as shown in Table , for e-NAND. As long as the e-NAND is busy, the corresponding bit (31) is set to LOW, the ‘wired-and’ operation, described in Chapter 4.2.2 yields LOW, if at least one e-NAND is still busy.

3.4.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the e-NAND identification information used during the card identification phase (e-NAND protocol). Every individual flash or e-NAND shall have an unique identification number. The MSB bytes of the register contain manufacturer data and two least significant bytes contains the host controlled data - the card Copy and write protection and the user ECC register. Every type of e-NAND ROM cards (defined by content) shall have an unique identification number.
The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice	CID Value	COMMENT
Manufacturer ID	MID	8	[127:120]	0x90	Hynix Manufacture ID
Reserved		6	[119:114]	-	
Card/BGA	CBX	2	[113:112]	01b	
OEM/Application ID	OID	8	[111:104]	0x4A	
Product name	PNM	48	[103:56]	HYNIX	6 ASCII characters
Product revision	PRV	8	[55:48]	0x01	
Product serial number	PSN	32	[47:16]	random number	
Manufacturing date	MDT	8	[15:8]	6C	
CRC7 checksum	CRC	7	[7:1]	2b	
not used, always '1'	-	1	[0:0]	1	

a. They will be changed by manufacturing data and contents. All values are not fixed yet. Please refer to current value

Table 3-8 : The CID fields

● **MID**

An 8 bit binary number that identifies the manufacturer. The MID number is controlled, defined and allocated to a e-NAND manufacturer by the MMCA. This procedure is established to ensure uniqueness of the CID register.

● **CBX**

CBX indicates the device type.

[113:112]	Type
00	Card(removable)
01	BGA(embedded)
10, 11	Reserved

● **OID**

A 8 bit binary number that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a e-NAND manufacturer by the MMCA. This procedure is established to ensure uniqueness of the CID register.

● **PNM**

The product name is a string, 6 ASCII characters long.

● **PRV**

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an n.m revision

number. The n is the most significant nibble and m is the least significant nibble.

As an example, the PRV binary value field for product revision 6.2 will be: 0110 0010

● **PSN**

A 32 bits unsigned binary integer.

● **MDT**

The manufacturing date is composed of two hexadecimal digits, four bits each, representing a two digits date code m/y; The m field, most significant nibble, is the month code. 1 = January.

The y field, least significant nibble, is the year code. 0 = 1997.

As an example, the binary value of the MDT field for production date April 2000 will be: 0100 0011

● **CRC**

CRC7 checksum (7 bits). This is the checksum of the CID contents computed according to Chapter 6.4.

3.4.3 CSD Register

The Card-Specific Data register provides information on how to access the e-NAND contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:

R = readable, W = writable once, E = erasable (multiple writable).

Name	Field	Width	Cell Type	CSDslice	CSD Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	2
System specification version	SPEC_VERS	4	R	[125:122]	4
Reserved	-	2	R	[121:120]	0
Data read access-time 1	TAAC	8	R	[119:112]	4F
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32
e-NAND command classes	CCC	12	R	[95:84]	F5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	1
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0
DSR implemented	DSR_IMP	1	R	[76:76]	0
Reserved	-	2	R	[75:74]	0
Device size	C_SIZE	12	R	[73:62]	F0F
Max. read current @ V_{ccq} min	V_{ccq}_R_CURR_MIN	3	R	[61:59]	7
Max. read current @ V_{ccq} max	V_{ccq}_R_CURR_MAX	3	R	[58:56]	7
Max. write current @ V_{ccq} min	V_{ccq}_W_CURR_MIN	3	R	[55:53]	7
Max. write current @ V_{ccq} max	V_{ccq}_W_CURR_MAX	3	R	[52:50]	7
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	1
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0
Write speed factor	R2W_FACTOR	3	R	[28:26]	2
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	a
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0
Reserved	-	4	R	[20:17]	0
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0
Copy flag (OTP)	COPY	1	R/W	[14:14]	0
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0
File format	FILE_FORMAT	2	R/W	[11:10]	0
ECC code	ECC	2	R/W/E	[9:8]	0
CRC	CRC	7	R/W/E	[7:1]	4d
Not used, always '1'	-	1	-	[0:0]	1

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

● **CSD_STRUCTURE**

Describes the version of the CSD structure.

CSD_STRUCTURE	CSD structure version	Valid for System Specification Version
0	CSD version No. 1.0	Allocated by MMCA
1	CSD version No. 1.1	Allocated by MMCA
2	CSD version No. 1.2	Version 4.1 - 4.2 - 4.3
3	Version is coded in the CSD_STRUCTURE byte in the EXT_CSD register	

● **SPEC_VERS**

Defines the JEDEC JESD84 V4.3 series of specifications supported by the e-NAND.

SPEC_VERS	System Specification Version Number
0	Allocated by MMCA
1	Allocated by MMCA
2	Allocated by MMCA
3	Allocated by MMCA
4	Version 4.1 - 4.2 -4.3
5 - 15	Reserved

● **TAAC**

Defines the asynchronous part of the data access time.

TAAC bit position	code
2:0	Time unit 0=1ns, 1=10ns, 2=100ns, 3=1µs, 4=10µs, 5=100µs, 6=1ms, 7=10ms
6:3	Multiplier factor 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	Reserved

● **NSAC**

Defines the typical case for the clock dependent factor of the data access time. The unit for NSAC is 100 clock cycles. Therefore, the maximal value for the clock dependent part of the data access time is 25.5k clock cycles.
The total access time NAC as expressed in Table TAAC is calculated based on TAAC and NSAC. It has to be computed by the host for the actual clock rate. The read access time should be interpreted as a typical delay for the first data bit of a data block or stream.

● **TRAN_SPEED**

The following table defines the clock frequency when not in high speed mode. For e-NAN supporting version 4.3, the value shall be
26 MHz (0x32).

TAAC bit position	code
2:0	Frequency unit 0=100KHz, 1=1MHz, 2=10MHz, 3=100MHz, 4...7=reserved
6:3	Multiplier factor 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.6, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.2, C=5.5, D=6.0, E=7.0, F=8.0
7	Reserved

● **CCC**

The e-NAND command set is divided into subsets (command classes). The e-NAND command class register CCC defines which command classes are supported by this card. A value of 1 in a CCC bit means that the corresponding command class is supported. For command class definition refer to Table 4-8.

CCC bit	Supported card command class
0	class 0
1	class 1
.....	
11	class 11

● **READ_BL_LEN**

The data block length is computed as 2READ_BL_LEN. The block length might therefore be in the range 1B, 2B,4B...16kB. bytes (see Chapter 4.10 for details):

READ_BL_LEN		Supported card command class
0	2^0 = 1 Byte	
1	2^1 = 2 Bytes	
.....		
11	2^{11} = 2048 Bytes	
12	2^{12} = 4096 Bytes	
13	2^{13} = 8192 Bytes	
14	2^{14} = 16 Kbytes	
15	2^{15} =Extention	New register TBD to EXT_CSD

- **READ_BL_PARTIAL**

Defines whether partial block sizes can be used in block read commands.
Up to 2GB of density (byte access mode):
READ_BL_PARTIAL=0 means that only the 512B and the READ_BL_LEN block size can be used for block oriented data transfers.
READ_BL_PARTIAL=1 means that smaller blocks can be used as well. The minimum block size will be equal to minimum addressable unit (one byte).
Higher than 2GB of density (sector access mode):
READ_BL_PARTIAL=0 means that only the 512B and the READ_BL_LEN block sizes can be used for block oriented data transfers.
READ_BL_PARTIAL=1 means that smaller blocks than indicated in READ_BL_LEN can be used as well. The minimum block size will be equal to minimum addressable unit, one sector (512B).

WRITE_BLK_MISALIGN

Defines if the data block to be written by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in WRITE_BL_LEN.
WRITE_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.
WRITE_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

READ_BLK_MISALIGN

Defines if the data block to be read by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in READ_BL_LEN.
READ_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.
READ_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

DSR_IMP

Defines if the configurable driver stage is integrated on the e-NAND. If set, a driver stage register (DSR) must be implemented also (see Chapter 3.5.6).

DSR_IMP	DSR type
0	DSR is not implemented
1	DSR implemented

- **C_SIZE**

This parameter is used to compute the e-NAND capacity. The memory capacity of the e-NAND is computed from the entries C_SIZE, C_SIZE_MULT and READ_BL_LEN as follows:
e-NAND capacity = BLOCKNR * BLOCK_LEN
where

BLOCKNR = (C_SIZE+1) * MULT

MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)

BLOCK_LEN = $2^{READ\_BL\_LEN}$, (READ_BL_LEN < 12)

Therefore, the maximal capacity which can be coded is 4096*512*2048 = 4 GBytes. Example: A 4 MByte e-NAND with BLOCK_LEN = 512 can be coded by C_SIZE_MULT = 0 and C_SIZE = 2047.

- **Vccq_R_CURR_MIN, Vccq_W_CURR_MIN**

The maximum values for read and write currents at the minimal power supply V_{ccq} are coded as follows:

Vccq_R_CURR_MIN **Vccq_W_CURR_MIN**	Code for current consumption @ Vccq
2:0	0=0.5mA; 1=1mA; 2=5mA; 3=10mA; 4=25mA; 5=35mA; 6=60mA; 7=100mA

The values in these fields are valid when the vccq is not in high speed mode. When the vccq is in high speed mode, the current consumption is chosen by the host, from the power classes defined in the PWR_ff_vvv registers, in the EXT_CSD register.

● **Vccq_R_CURR_MAX, Vccq_W_CURR_MAX**

The maximum values for read and write currents at the maximal power supply Vccq are coded as follows:

Vccq_R_CURR_MIN **Vccq_W_CURR_MIN**	Code for current consumption @ V_{ccq}
2:0	0=1mA; 1=5mA; 2=10mA; 3=25mA; 4=35mA; 5=45mA; 6=80mA; 7=200mA

The values in these fields are valid when the e-NAND is not in high speed mode. When the e-NAND is in high speed mode, the current consumption is chosen by the host, from the power classes defined in the PWR_ff_vvv registers, in the EXT_CSD register.

C_SIZE_MULT

This parameter is used for coding a factor MULT for computing the total device size (see C_SIZE). The factor MULT is defined as $2^{C\_SIZE\_MULT+2}$.

C_SIZE_MULT	MULT
0	$2^2 = 4$
1	$2^3 = 8$
2	$2^4 = 16$
3	$2^5 = 32$
4	$2^6 = 64$
5	$2^7 = 128$
6	$2^8 = 256$
7	$2^9 = 512$

● **ERASE_GRP_SIZE**

The contents of this register is a 5 bit binary coded value, used to calculate the size of the erasable unit of the e-NAND. The size of the erase unit (also referred to as erase group) is determined by the ERASE_GRP_SIZE and the ERASE_GRP_MULT entries of the CSD, using the following equation:
size of erasable unit = (ERASE_GRP_SIZE + 1) * (ERASE_GRP_MULT + 1)
This size is given as minimum number of write blocks that can be erased in a single erase command.

● **ERASE_GRP_MULT**

A 5 bit binary coded value used for calculating the size of the erasable unit of the e-NAND. See ERASE_GRP_SIZE section for detailed description.

● **WP_GRP_SIZE**

The size of a write protected group. The contents of this register is a 5 bit binary coded value, defining the number of erase groups which can be write protected. The actual size is computed by increasing this number by one. A value of zero means 1 erase group, 31 means 32 erase groups.

- **WP_GRP_ENABLE**

A value of 0 means no group write protection possible.

- **DEFAULT_ECC**

Set by the manufacturer. It defines the ECC code which is recommended for use. The field definition is the same as for the ECC field described later.

- **R2W_FACTOR**

Defines the typical block program time as a multiple of the read access time. The following table defines the field format.

C_SIZE_MULT	Multiples of read access time
0	1
1	2 (write half as fast as read)
2	4
3	8
4	16
5	32
6	64
7	128

- **WRITE_BL_LEN**

Block length for write operations. See READ_BL_LEN for field coding.
Note that the support for 512B write access is mandatory for all cards. And that the cards has to be in 512B block length mode by default after power-on, or software reset. The purpose of this register is to indicate the supported maximum write data block length.

- **WRITE_BL_PARTIAL**

Defines whether partial block sizes can be used in block write commands.
Up to 2GB of density (byte access mode):
WRITE_BL_PARTIAL='0' means that only the 512B and the WRITE_BL_LEN block size can be used for block oriented data write.
WRITE_BL_PARTIAL='1' means that smaller blocks can be used as well. The minimum block size is one byte.
Higher than 2GB of density (sector access mode):
WRITE_BL_PARTIAL='0' means that only the 512B and the WRITE_BL_LEN block size can be used for block oriented data write.
WRITE_BL_PARTIAL='1' means that smaller blocks can be used as well. The minimum block size will be equal to minimum addressable unit, one sector (512B).

- **FILE_FORMAT_GRP**

Indicates the selected group of file formats. This field is read-only for ROM. The usage of this field is shown in Table 3-25(see FILE_FORMAT).

- **COPY**

Defines if the contents is original (= 0) or has been copied (=1). The COPY bit for OTP and MTP devices, sold to end consumers, is set to 1 which identifies the card contents as a copy. The COPY bit is an one time programmable bit.

- **PERM_WRITE_PROTECT**

Permanently protects the whole card content against overwriting or erasing (all write and erase commands for this card are permanently disabled). The default value is 0, i.e. not permanently write protected.

- **TMP_WRITE_PROTECT**

Temporarily protects the whole card content from being overwritten or erased (all write and erase commands for card are temporarily disabled). This bit can be set and reset. The default value is 0, i.e. not write protected.

- **CONTENT_PROT_APP**

This field in the CSD indicates whether the content protection application is supported. e-NAND which implement the content protection application will have this bit set to 1;

- **FILE_FORMAT**

Indicates the file format on the card. This field is read-only for ROM. The following formats are defined:

FILE_FORMAT_GRP	FILE_FORMAT	Type
0	0	Hard disk-like file system with partition table
0	1	DOS FAT (floppy-like) with boot sector only (no partition table)
0	2	Universal File Format
0	3	Others / Unknown
1	0,1,2,3	Reserved

A more detailed description is given in "File Formats Specifications For e-NAND".

- **ECC**

Defines the ECC code that was used for storing data on the card. This field is used by the host (or application) to decode the user data. The following table defines the field format.:

ECC	FILE_FORMAT	Maximum number of correctable bits per block
0	None (default)	none
1	BCH (542,512)	3
2,3	reserved	-

- **CRC**

The CRC field carries the check sum for the CSD contents. It is computed according to Chapter 6.4. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

The following table lists the correspondence between the CSD entries and the command classes. A '+' entry indicates that the CSD field affects the commands of the related command class.

	Command classes									
CSD Field	0	1	2	3	4	5	6	7	8	9
CSD_STRUCTURE	+	+	+	+	+	+	+	+	+	+
SPEC_VERS	+	+	+	+	+	+	+	+	+	+
TAAC		+	+	+	+	+	+	+	+	
NSAC		+	+	+	+	+	+	+	+	
TRAN_SPEED		+	+	+	+					
CCC	+	+	+	+	+	+	+	+	+	+
READ_BL_LEN			+							
READ_BL_PARTIAL			+							
WRITE_BLK_MISALIGN					+					
READ_BLK_MISALIGN			+							
DSR_IMP	+	+	+	+	+	+	+	+	+	+
C_SIZE_MANT		+	+	+	+	+	+	+	+	
C_SIZE_EXP		+	+	+	+	+	+	+	+	
Vccq_R_CURR_MIN		+	+							
Vccq_R_CURR_MAX		+	+							
Vccq_W_CURR_MIN				+	+	+	+	+	+	
Vccq_W_CURR_MAX				+	+	+	+	+	+	
ERASE_GRP_SIZE						+	+	+	+	
WP_GRP_SIZE							+	+	+	
WP_GRP_ENABLE							+	+	+	
DEFAULT_ECC		+	+	+	+	+	+	+	+	
R2W_FACTOR				+	+	+	+	+	+	
WRITE_BL_LEN				+	+	+	+	+	+	
WRITE_BL_PARTIAL				+	+	+	+	+	+	
FILE_FORMAT_GRP										
COPY	+	+	+	+	+	+	+	+	+	+
PERM_WRITE_PROTECT	+	+	+	+	+	+	+	+	+	+
TMP_WRITE_PROTECT	+	+	+	+	+	+	+	+	+	+
FILE_FORMAT										
ECC		+	+	+	+	+	+	+	+	
CRC	+	+	+	+	+	+	+	+	+	+

3.4.4 Extended CSD Register

The Extended CSD register defines the e-NAND properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e-NAND capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e-NAND is working in. These modes can be changed by the host by means of the SWITCH command

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Reserved value
Properties Segment					
Reserved[1]		7		[511:505]	
Supported Command Sets	S_CMD_SET	1	R	[504]	1
Reserved[1]		275	TBD	[503:229]	
Boot information	BOOT_INFO	1	R	[228]	1
Reserved[1]		1	TBD	[227]	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	2
Access size	ACC_SIZE	1	R	[225]	0
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0
Reliable write sector count	REL_WR_SEC_C		R	[222]	1
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0
Sleep current(VCC)	S_C_VCC	1	R	[220]	04h
Sleep current(VCCQ)	S_C_VCCQ	1	R	[219]	08h
Reserved[1]		1	TBD	[218]	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0Bh
Reserved[1]		1	TBD	[216]	0
Sector Count	SEC_COUNT	4	R	[215:212]	0
Reserved[1]		1		[211]	
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	08h
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	08h
Minimum Write Performance for 8bit @26MHz / 4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	08h

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Reserved value
Minimum Read Performance for 8bit @26MHz / 4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[207]	08h
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	08h
Minimum Read Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[205]	08h
Reserved[1]		1	R	[204]	
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	0
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	0
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	0
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	0
Reserved[1]		3		[199:197]	
Card Type	CARD_TYPE	1	R	[196]	3
Reserved[1]		1		[195]	
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	2
Reserved[1]		1		[193]	
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	03h
Command Set	CMD_SET	1	R/W	[191]	0
Reserved[1]		1		[190]	
Command Set Revision	CMD_SET_REV	1	RO	[189]	0
Reserved[1]		1		[188]	
Power Class	POWER_CLASS	1	R/W	[187]	0
Reserved[1]		1		[186]	
High Speed Interface Timing	HS_TIMING	1	R/W	[185]	0
Reserved[1]		1		[184]	
Bus Width Mode	BUS_WIDTH	1	WO	[183]	1
Reserved[1]		1		[182]	

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Reserved value
Erased Memory Content	ERASED_MEM_CONT	1	RO	[1817]	0
Reserved1		1		[180]	
Boot configuration	BOOT_CONFIG	1	R/W	[179]	0
Reserved[1]		1		[178]	
Boot bus width	BOOT_BUS_WODTH	1	R/W	[177]	0
Reserved[1]		1		[176]	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W	[175]	0
Reserved[1]		175		[174:0]	

NOTE :
1. Reserved bits should read as '0'

Table 3-27 : Extended CSD

● **S_CMD_SET**
This field defines which command sets are supported by the e-NAND.

Bit	Command Set
7-5	Reserved
4	Allocated by MMCA
3	Allocated by MMCA
2	Allocated by MMCA
1	Allocated by MMCA
0	Standard MMC

● **BOOT_INFO**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							ALT_BOOT_MODE

Bit[7:1]: Reserved
Bit[0]: ALT_BOOT_MODE
0: Device does not support alternate boot met
1: Device supports alternate boot method.

● **BOOT_SIZE_MULT**

The boot partition size is calculated from the register by using the following equation:

Boot partition size 128Kbytes BOOT_SIZE_MULT

Value	Timeout Values
0x00	No boot partition available / Boot mode not supported
0x01	1 x 128Kbytes = 128Kbytes
0x02	2 x 128Kbytes = 256Kbytes
:	:
0xFE	254 x 128Kbytes = 32512Kbytes
0xFF	255 x 128Kbytes =32640Kbytes

● **ACC_SIZE**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				SUPER_PAGE_SIZE			

Bit[7:4]: Reserved
Bit[3:0]: SUPER_PAGE_SIZE
This register defines one or multiple of programmable boundary unit which is programmed at the same time. This value can be used by the master for the following cases:
As a guide for format clusters
To prevent format-page misalignment
As a guide for minimum data-transfer size
Super-page size = 512 × 2(SUPER_PAGE_SIZE - 1) : 0 < X < 9

Value	Timeout Values
0x0	Not defined
0x1	512 x 1 = 512bytes
0x2	512 x 1 = 1K bytes
:	:
0x8	512 x 128 = 64K bytes
0x9-0xF	Reserved

- **HC_ERASE_GRP_SIZE**

This register defines the erase-unit size for high-capacity memory. If the master enables bit "0" in the extended CSD register byte [175], the slave uses these value for the erase operation.
Erase Unit Size = 512Kbyte × HC_ERASE_GRP_SIZE

Value	Timeout Values
0x0	No support for high-capacity erase-unit size
0x1	512Kbyte x 1 = 524,288 bytes
0x2	512Kbyte x 1 = 1,048,576 bytes
:	:
0xFF	512Kbyte x 1 = 133,693,440 bytes

If the ENABLE bit in ERASE_GROUP_DEF is cleared to LOW or HC_WP_GRP_SIZE is set to 0x00, the write protect group size definition would be the original case.

- **ERASE_TIMEOUT_MULT**

This register is used to calculate erase timeout for high-capacity erase operations and defines the timeout value for the erase operation of one erase group.
Erase Timeout = 300ms × ERASE_TIMEOUT_MULT
If the host executes erase operations for multiple erase groups, the total timeout value should be the multiple of the number of erase groups issued.
If the master enables bit 0 in the extended CSD register byte [175], the slave uses
ERASE_TIMEOUT_MULT values for the timeout value.
If ERASE_TIMEOUT_MULT is set to 0x00, the slave must support the previous timeout definition.

Value	Timeout Values
0x00	No support for high-capacity erase timeout
0x01	300ms x 1 = 300ms
0x02	300ms x 2 = 600ms
:	:
0xFF	300ms x 255 = 76,500ms

● **REL_WR_SEC_C**

The reliable write feature requires mandatory sector count 1 (512B) support.

With this register it is also possible to indicate an additional supported sector count.

In applications where only the single-sector write is supported, the value in the register should be "1." Otherwise, the value should be the multiple of the number of sectors supported.

Name	Field	Size	Cell Type
Reliable Write Sector Count	REL_WR_SEC_C	1	R

● **HC_WP_GRP_SIZE**

This register defines the write protect group size for high-capacity memory. If the ENABLE bit in ERASE_GROUP_DEF is set to HIGH, the write protect group size would be defined as follows:
Write protect group size = 512KB * HC_ERASE_GRP_SIZE * HC_WP_GRP_SIZE.

Value	Timeout Values
0x00	No support for high-capacity write protect group size
0x01	1 high-capacity erase unit size
0x02	2 high-capacity erase unit size
0x03	3 high-capacity erase unit size
:	:
0xFF	255 high-capacity erase unit size

If the ENABLE bit in ERASE_GROUP_DEF is cleared to LOW or HC_WP_GRP_SIZE is set to 0x00, the write protect group size definition would be the original case.

- **S_C_VCC, S_C_VCCQ**

The S_C_VCC and S_C_VCCQ registers define the max VCC current consumption during the Sleep state (slp). The formula to calculate the max current value is:

Sleep current = 1µA * 2x : register value = X >0

Sleep current = no value (legacy) : register value = 0

Max register value defined is 0x0D which equals 8.192mA. Values between 0x0E and 0xFF are reserved.

Value	Value definition
0x00	Not defined
0x01	1uA x 2^1= 2uA
0x02	1uA x 2^2 = 4uA
:	:
0x17	1uA x 2^{13} = 8.192mA
0x18-0xFF	Reserved

- **S_A_TIMEOUT**

This register defines the max timeout value for state transitions from Standby state (stby) to Sleep state (slp) and from Sleep state (slp) to Standby state (stby). The formula to calculate the max timeout value is:

Sleep/Awake Timeout = 100ns * 2S_A_timeout

Max register value defined is 0x17 which equals 838.86ms timeout. Values between 0x18 and 0xFF are reserved.

Value	Value definition
0x00	Not defined
0x01	100ns x 2^1= 200ns
0x02	100ns x 2^2 = 400ns
:	:
0x17	100ns x 2^{23} = 838.86ns
0x18-0xFF	Reserved

- **SEC_COUNT**

The device density is calculated from the register by multiplying the value of the register (sector count) by 512B/sector. The maximum density possible to be indicated is thus 2 Tera bytes (4 294 967 296 x 512B). The least significant byte (LSB) of the sector count value is the byte [212].

● **MIN_PERF_a_b_ff**

These fields defines the overall minimum performance value for the read and write access with different bus width and max clock frequency modes. The value in the register is coded as follows. Other than defined values are illegal.

Value	Value definition
0x00	For cards not reaching the 2.4MB/s value
0x08	Class A : 2.4MB/s and is the next allowed value(16x150kB/s)
0x0A	Class A : 2.4MB/s and is the next allowed value(16x150kB/s)
0x0F	Class C : 4.5MB/s and is the next allowed value(30x150kB/
0x14	Class D : 6.0MB/s and is the next allowed value(40x150kB/s)
0x1E	Class E : 9.0MB/s and is the next allowed value(60x150kB/s) This is also the highest class which any MMCplus or MMC mobile card is needed to support in low bus category operation mode (26MHz with 4bit data bus). A MMCplus or MMCmobile card supporting any higher class than this have to support this class also (in low category bus operation mode).
0x28	Class D : 12.0MB/s and is the next allowed value(80x150kB/s)
0x32	Class D : 15.0MB/s and is the next allowed value(100x150kB/s)
0x3C	Class D : 18.0MB/s and is the next allowed value(120x150kB/s)
0x46	Class D : 21.0MB/s and is the next allowed value(140x150kB/s) This is also the highest class which any MMCplus or MMC mobile card is needed to support in mid bus category operation mode (26MHz with 8bit data bus or 52MHz with 4bit data bus). A MMCplus or MMCmobile card supporting any higher class than this have to support this Class (in mid category bus operation mode) and Class E also (in low category bus operation mode)
0x50	Class D : 24.0MB/s and is the next allowed value(160x150kB/s)
0x64	Class D : 30.0MB/s and is the next allowed value(200x150kB/s)
0x78	Class D : 36.0MB/s and is the next allowed value(240x150kB/s)
0x8C	Class D : 42.0MB/s and is the next allowed value(280x150kB/s)
0x40	Class D : 48.0MB/s and is the last defined value(320x150kB/s)

● **PWR_CL_ff_vvv**

These fields define the supported power classes by the e-NAND. By default, the e-NAND has to operate at maximum frequency using 1 bit bus configuration, within the default max current consumption, as stated in the table below. If 4 bit/8 bits bus configurations, require increased current consumption, it has to be stated in these registers.
By reading these registers the host can determine the power consumption of the e-NAND in different bus modes. Bits [7:4] code the current consumption for the 8 bit bus configuration. Bits [3:0] code the current consumption for the 4 bit bus configuration The PWR_52_vvv registers are not defined for 26MHz e-NAND.

Voltage	Value	Max RMS Current	Max Peak Current	Remarks
3.6V	0	100 mA	200 mA	Default current consumption for high voltage cards
	1	120 mA	220 mA	
	2	150 mA	250 mA	
	3	180 mA	280 mA	
	4	200 mA	300 mA	
	5	220 mA	320 mA	
	6	250 mA	350 mA	
	7	300 mA	400 mA	
	8	350 mA	450 mA	
	9	400 mA	500 mA	
	10	450 mA	550 mA	
	11-15			Reserved for future use

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.
Max peak current is defined as absolute max value not to be exceeded at all.
The conditions under which the power classes are defined are:

- Maximum bus frequency
- Maximum operating voltage
- Worst case functional operation
- Worst case environmental parameters (temperature,...)

These registers define the maximum power consumption for any protocol operation in data transfer mode, Ready state and Identification state.

- **CARD_TYPE**

This field defines the type of the e-NAND. The only currently valid values for this field are 0x01 and 0x03.

Bit	Card Type
7:2	Reserved
1	High Speed e-NAND @ 52MHz
0	High Speed e-NAND @ 26MHz

- **CSD_STRUCTURE**

This field is a continuation of the CSD_STRUCTURE field in the CSD register

CSD_STRUCTURE	CSD structure version	Valid for System Specification Version
0	CSD version No. 1.0	Allocated by MMCA
1	CSD version No. 1.1	Allocated by MMCA
2	CSD version No. 1.2	Version 4.1- 4.2 - 4.3
3-255	Reserved for future use	

- **EXT_CSD_REV**

Defines the fixed parameters. related to the EXT_CSD, according to its revision

EXT_CSD_REV	Extended CSD Revision
255-4	Reserved
3	Revision 1.3
2	Revision 1.2
1	Revision 1.1
0	Revision 1.0

- **CMD_SET**

Contains the binary code of the command set that is currently active in the card. It is set to 0 (Standard MMC) after power up and can be changed by a SWITCH command. Note that while changing the command set with the SWITCH command, bit index values according to the S_CMD_SET register should be used. For backward compatibility, the CMD_SET is set to 0x00 (standard MMC) following power-up. After switching back to the standard MMC command set with the SWITCH command, the value of the CMD_SET is 0x01.

- **CMD_SET_REV**

Contains a binary number reflecting the revision of the currently active command set. For Standard MMC. command set it is:

Code	MMC Revisions
255-1	Reserved
0	v4.0

This field, though in the Modes segment of the EXT_CSD, is read only.

- **POWER_CLASS**

Bits	Description
[7:4]	Reserved
[3:0]	Card power class code (See Table 3-2)

- **HS_TIMING**

This field is 0 after power-on, or software reset, thus selecting the backwards compatibility interface timing for the e-NAND. If the host writes 1 to this field, the e-NAND changes its timing to high speed interface timing

- **BUS_WIDTH**

It is set to 0 (1 bit data bus) after power up and can be changed by a SWITCH command.

Value	Bus Mode
255-3	Reserved
2	8 bit data bus
1	4 bit data bus
0	1 bit data bus

- **ERASED_MEM_CONT**

This field defines the content of an explicitly erased memory range.

Value	Erased Memory Content
255-2	Reserved
1	Erased memory range shall be '1'
2	Erased memory range shall be '0'

● **BOOT_CONFIG**
This register defines the configuration for boot operation.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BOOT_ACK	BOOT_PARTITION_ENABLE			BOOT_PARTITION_ACCESS		

Bit 7: Reserved
Bit 6: BOOT_ACK (non-volatile)
0x0 : No boot acknowledge sent (default)
0x1 : Boot acknowledge sent during boot operation
Bit[5:3] : BOOT_PARTITION_ENABLE (non-volatile)
User selects boot data that will be sent to master
0x0 : Device not boot enabled (default)
0x1 : Boot partition 1 enabled for boot
0x2 : Boot partition 2 enabled for boot
0x3–0x6 : Reserved
0x7 : User area enabled for boot
Bit[2:0] : BOOT_PARTITION_ACCESS
User selects boot partition for read and write operation
0x0 : No access to boot partition (default)
0x1 : R/W boot partition 1
0x2 : R/W boot partition 2
0x3–0x7 : Reserved

● **BOOT_BUS_WIDTH**
This register defines the configuration for boot operation.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					RESET_BOOT_BUS_WIDTH	BOOT_BUS_WIDTH	

Bit[7:3] : Reserved
Bit 2: RESET_BOOT_BUS_WIDTH (non-volatile)
0x0 : Reset bus width to x1 after boot operation (default)
0x1 : Retain boot bus width after boot operation
Bit[1:0] : BOOT_BUS_WIDTH (non-volatile)
0x0 : x1 bus width in boot operation mode (default)
0x1 : x4 bus width in boot operation mode
0x2 : x8 bus width in boot operation mode
0x3 : Reserved

● **ERASE_GROUP_DEF**

This register allows master to select high capacity erase unit size, timeout value, and write protect group size. Bit defaults to "0" on power on.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							ENABLE

Bit[7:1]: Reserved
Bit0: ENABLE
0x0 : Use old erase group size and write protect group size definition (default)
0x1 : Use high-capacity erase unit size, high capacity erase timeout, and high-capacity write protect group size definition.

3.4.5 RCA Register

The writable 16-bit relative e-NAND address register carries the e-NAND address assigned by the host during the e-NAND identification. This address is used for the addressed host-e-NAND communication after the e-NAND identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all e-NAND into the Stand-by State with CMD7.

3.4.6 DSR Register

The 16-bit driver stage register can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

4. e-NAND Protocol Description

All communication between host and e-NAND is controlled by the host (master). The host sends commands of two types:
broadcast and addressed (point-to-point) commands.

- Broadcast commands : Broadcast commands are intended for e-NAND in a MMC Card system[1]. Some of these commands require a response.
- Addressed (point-to-point) commands : The addressed commands are sent to the addressed e-NAND and cause a response from this e-NAND.

A general overview of the command flow is shown in Figure 4-1 for the e-NAND identification mode and in Figure 4-2 for the data transfer mode. The commands are listed in the command tables (Table 4-8 - Table 4-17). The dependencies between current state, received command and following state are listed in Table 4-18. In the following sections, the different card operation modes are described first. Thereafter, the restrictions for controlling the clock signal are defined. All e-NAND commands together with the corresponding responses, state transitions, error conditions and timings are presented in the succeeding sections.
Three operation modes are defined for the e-NAND system (hosts and e-NAND):

- Card identification mode
  The host will be in e-NAND identification mode after reset, while it is looking for a e-NAND on the bus.
  The e-NAND will be in this mode after reset, until the SET_RCA command (CMD3) is received.
- Interrupt mode
  Host and e-NAND enter and exit interrupt mode simultaneously. In interrupt mode there is no data transfer. The only mes sage allowed is an interrupt service request from the e-NAND or the host.
- Data transfer mode
  The e-NAND will enter data transfer mode once an RCA is assigned to it. The host will enter data transfer mode after identifying the e-NAND on the bus.

The following table shows the dependencies between bus modes, operation modes and e-NAND states. Each state in the e-NAND state diagram (see Figure 4-5 and Figure 4-6) is associated with one bus mode and one operation mode:

Card state	Operation mode	Bus mode
Inactive State	Inactive	Open-drain
Pre-Idle State	Boot mode	
Pre-Boot State		
Idle State	e-NAND identification mode	
Ready State		
Identification State		
Stand-by State	Data transfer mode	Push-pull
Sleep State		
Transfer State		
Bus-Test State		
Sending-data State		
Receive-data State		
Programming State		
Disconnect State		

Card state	Operation mode	Bus mode
Boot State	Boot mode	Push-pull
Wait-IRQ State	Interrupt mode	Open-drain

1.Broadcast commands are kept for backwards compatibility to previous MMC Card systems, where more than one e-NAND was allowed on the bus.

4.1 Boot operation mode

In boot operation mode, the master (e-NAND host) can read boot data from the slave(MMC device) by keeping CMD line low after power-on, or sending CMD0 with argument + 0xFFFFFFFA(optional for slave), before issuing CMD1. The data can be read from either boot area or user area depending on register setting.

4.1.1 Boot partition

There are two partition regions. The minimum size of each boot partition is 128KB. Boot partition size is calculated as follows:

Maximum boot partition size = 128K byte x BOOT_SIZE_MULT

BOOT_SIZE_MULT: the value in Extended CSD register byte [226]

The boot partitions are separated from the user area as shown in Figure 4-1 .

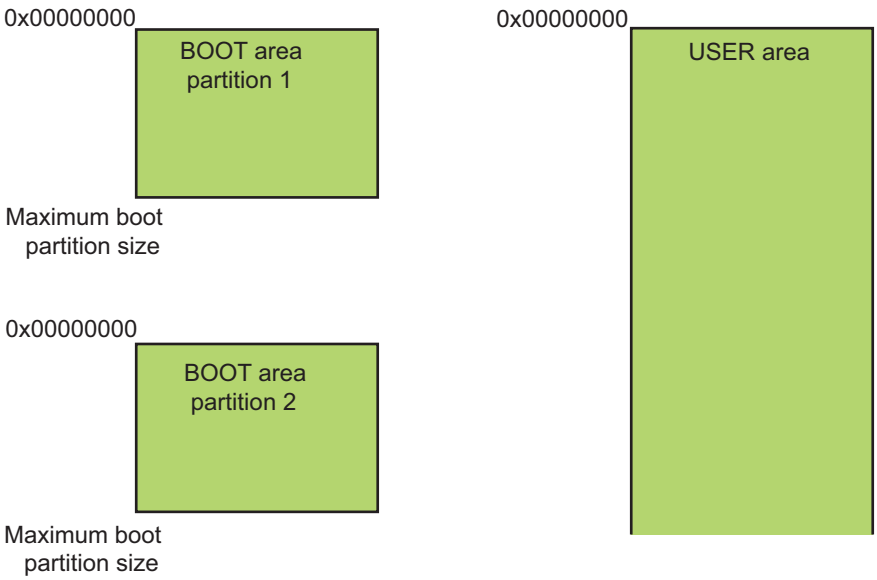


Figure 4-1: Memory partition

Slave has boot configuration in Extended CSD register byte [179]. The master can choose the configuration by setting the register using CMD6 (switch). Slave also can be configured to boot from the user area by setting the BOOT_PARTITION_ ENABLE bits in the EXT_CSD register, byte [179] to 111b

4.1.2 Boot operation

If the CMD line is held LOW for 74 clock cycles and more after power-up before the first command is issued, the slave recognizes that boot mode is being initiated and starts preparing boot data internally. The partition from which the master will read the boot data can be selected in advance using EXT_CSD byte 179, bits [5:3]. The data size that the master can read during boot operation can be calculated as 128KB × BOOT_SIZE_MULT (EXT_CSD byte 226). Within 1 second after the CMD line goes LOW, the slave starts to send the first boot data to the master on the DAT line(s). The master must keep the CMD line LOW to read all of the boot data. The master must use push-pull mode until boot operation is terminated.

The master can use the backward-compatible interface timing shown in Table 3-7.

The master can choose to receive boot acknowledge from the slave by setting "1" in EXT_CSD register, byte 179, bit 6, so that the master can recognize that the slave is operating in boot mode.

If boot acknowledge is enabled, the slave has to send acknowledge pattern "010" to the master within 50ms after the CMD line goes LOW. If boot acknowledge is disabled, the slave will not send out acknowledge pattern "0-1-0."

The master can terminate boot mode with the CMD line HIGH. If the master pulls the CMD line HIGH in the middle of data transfer, the slave has to terminate the data transfer or acknowledge pattern within NST clock cycles (one data cycle and end bit cycle). If the master terminates boot mode between consecutive blocks, the slave must release the data line(s) within NST clock cycles.

Boot operation will be terminated when all contents of the enabled boot data are sent to the master. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1.

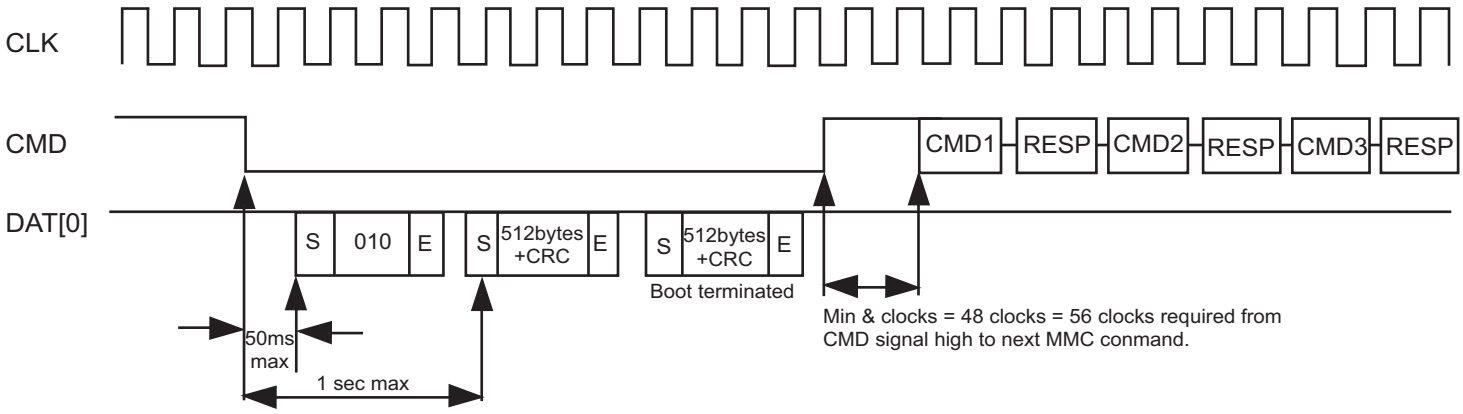
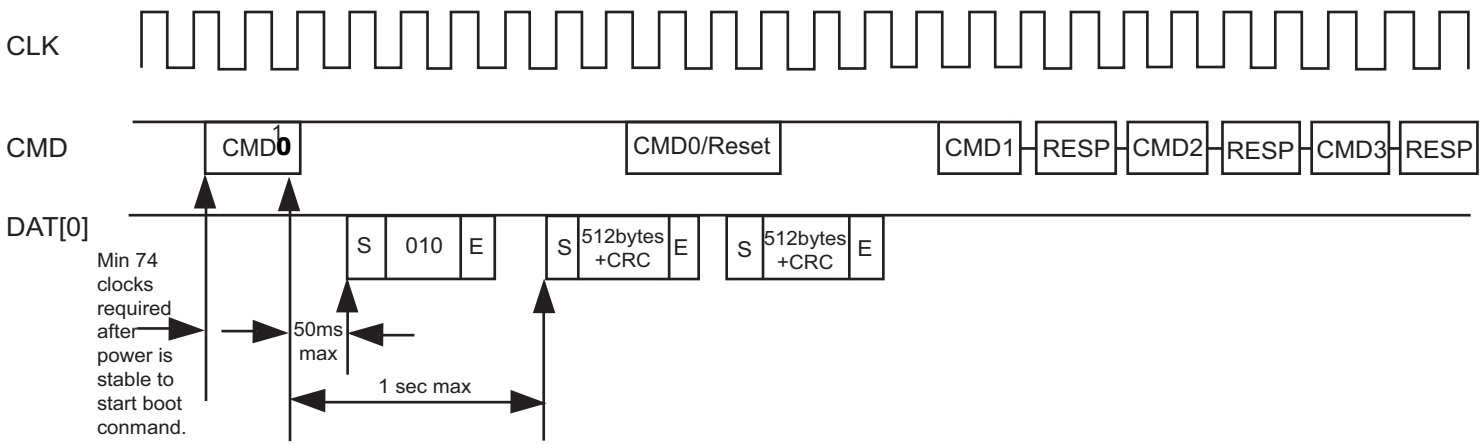


Figure 4-2: e-NAND state diagram (boot mode)

Detailed timings are shown in Section 4.17. Min 8 clocks + 48 clocks = 56 clocks required from CMD signal high to next MMC command.
If the CMD line is held LOW for less than 74 clock cycles after power-up before CMD1 is issued, or the master sends any normal MMC command other than CMD1 and CMD0 with argument 0xFFFFFFFA (if the device supports alternate boot operation) before initiating boot mode, the slave does not respond and will be locked out of boot mode until the next power cycle and enter Idle State.
When BOOT_PARTITION_ENABLE bits are set and master send CMD1 (SEND_OP_COND), slave must enter Card Identification Mode and respond to the command.
If the slave does not support boot operation mode, which is compliant with v4.2 or before, or BOOT_PARTITION_ENABLE bit is cleared, slave automatically enter Idle State after power-on.

4.1.3 Alternative boot operation (device optional)

This boot function is optional for the device. If bit 0 in the extended CSD byte[228] is set to "1," the device supports the alternative boot operation.
After power-up, if the host issues CMD0 with the argument of 0xFFFFFFFA after 74 clock cycles, before CMD1 is issued or the CMD line goes low, the slave recognizes that boot mode is being initiated and starts preparing boot data internally. The partition from which the master will read the boot data can be selected in advance using EXT_CSD byte 179, bits [5:3]. The data size that the master can read during boot operation can be calculated as 128KB × BOOT_SIZE_MULT (EXT_CSD byte 226. Within 1 second after CMD0 with the argument of 0xFFFFFFFA is issued, the slave starts to send the first boot data to the master on the DAT line(s). The master must use push-pull mode until boot operation is terminated. The master can use the backward-compatible interface timing shown in R2W_factor table on page 31.
The master can choose to receive boot acknowledge from the slave by setting "1" in EXT_CSD register, byte 179, bit 6, so that the master can recognize that the slave is operating in boot mode. If boot acknowledge is enabled, the slave has to send the acknowledge pattern "010" to the master within 50ms after the CMD0 with the argument of 0xFFFFFFFA is received. If boot acknowledge is disabled, the slave will not send out acknowledge pattern "010." The master can terminate boot mode by issuing CMD0 (Reset). If the master issues CMD0 (Reset) in the middle of a data transfer, the slave has to terminate the data transfer or acknowledge pattern within NST clock cycles (one data cycle and end bit cycle). If the master terminates boot mode between consecutive blocks, the slave must release the data line(s) within NST clock cycles.
Boot operation will be terminated when all contents of the enabled boot data are sent to the master. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1.sequence by sending CMD1.



NOTE 1. CMD0 with argument 0xFFFFFFFA

Figure 4-3: e-NAND state diagram (alternative boot mode)

Detailed timings are shown in Section 7.17.1..

If the CMD line is held LOW for less than 74 clock cycles after power-up before CMD1 is issued, or the master sends any normal MMC command other than CMD1 and CMD0 with argument 0xFFFFFFFA (if the device supports alternate boot operation) before initiating boot mode, the slave does not respond and will be locked out of boot mode until the next power cycle and enter Idle State.

When BOOT_PARTITION_ENABLE bits are set and master send CMD1 (SEND_OP_COND), slave must enter Card Identification Mode and respond to the command. If the slave does not support boot operation mode, which is compliant with v4.2 or before, or BOOT_PARTITION_ENABLE bit is cleared, slave automatically enter Idle State after power-on.

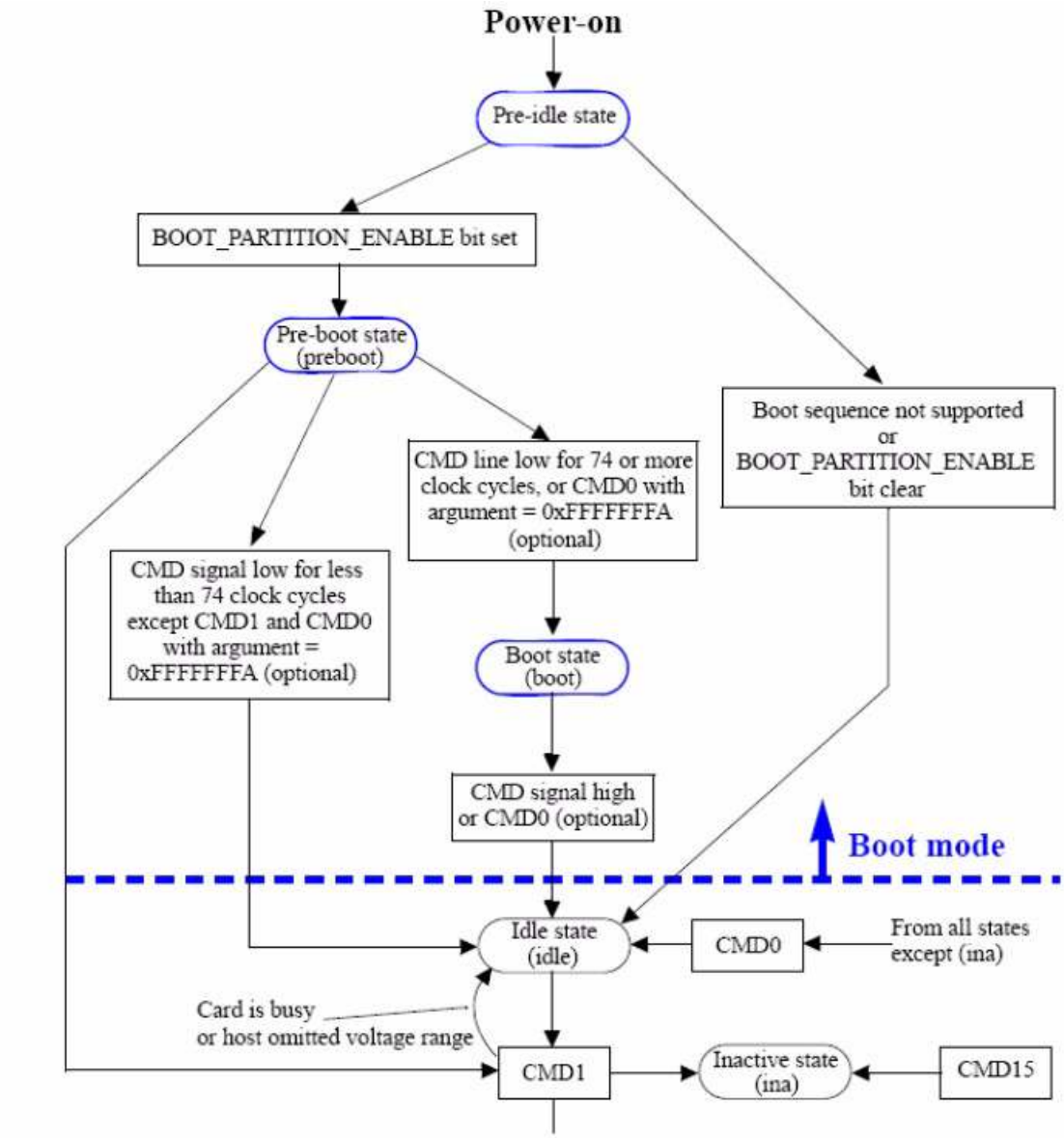


Figure 4-4: e-NAND state diagram (boot mode)

4.1.4 Access to boot partition

After putting a slave into transfer state, master sends CMD6 (SWITCH) to set the BOOT_PARTITION_ACCESS bits in the EXT_CSD register, byte [179]. After that, master can use normal MMC commands to access a boot partition.
Master can program boot data on DAT line(s) using CMD24 (WRITE_BLOCK) or CMD25 (WRITE_MULTIPLE_BLOCK) with slave supported addressing mode i.e. byte addressing or sector addressing. If the master uses CMD25 (WRITE_MULTIPLE_BLOCK) and the writes past the selected partition boundary, the slave will report an "ADDRESS_OUT_OF_RANGE" error. Data that is within the partition boundary will be written to the selected boot partition.
Master can read boot data on DAT line(s) using CMD17 (READ_SINGLE_BLOCK) or CMD18 (READ_MULTIPLE_BLOCK) with slave supported addressing mode i.e. byte addressing or sector addressing. If the master page uses CMD18 (READ_MULTIPLE_BLOCK) and then reads past the selected partition boundary, the slave will report an "ADDRESS_OUT_OF_RANGE" error. After finishing data access to the boot partition, the BOOT_PARTITION_ACCESS bits should be cleared. Then, non-volatile BOOT_PARTITION_ENABLE bits in the EXT_CSD register should be set to indicate which partition is enabled for booting. This will permit the slave to read data from the boot partition during boot operation.
Master also can access user area by using normal command by clearing BOOT_PARTITION_ACCESS bits in the EXT_CSD register, byte [179] to 000b.
If user area is locked and enabled for boot, data will not be sent out to master during boot operation mode. However, if the user area is locked and one of the two partitions is enabled, data will be sent out to the master during boot operation mode.

4.1.5 Boot bus width configuration

During boot operation, bus width can be configured by non-volatile configuration bits in the Extend CSD register byte[177] bit[0:1]. Bit2 in register byte[177] determines if the slave returns to x1 bus width after a boot operation or if it remains in the configured boot-bus width during normal operation. If boot operation is not executed, the slave will initialize in normal x1 bus width regardless of the register setting.

4.2 e-NAND Identification Mode

While in e-NAND identification mode the host resets the e-NAND, validates operation voltage range, identifies the e-NAND and assigns a Relative Card Address (RCA) to the e-NAND on the bus. All data communication in the e-NAND Identification Mode uses the command line (CMD) only.

4.2.1 Card Reset

After power-on by the host, the e-NAND (even if it has been in Inactive State) is in mode and in Idle State. Command GO_IDLE_STATE (CMD0) is the software reset command and puts the e-NAND into Idle State.
After power-on, or CMD0, the e-NAND output bus drivers are in high-impedance state and the e-NAND is initialized with a default relative e-NAND address („0x0001") and with a default driver stage register setting (lowest speed, highest driving current capability). The host clocks the bus at the identification clock rate fOD (see Chapter 3.3.10). CMD0 is valid in all states, with the exception of Inactive State . While in Inactive state the e-NAND does not accept CMD0.

4.2.2 Operating Voltage Range Validation

e-NAND shall be able to establish communication with the host, as well as perform the actual e-NAND function (e.g. accessing memory), using any operating voltage within the voltage range specified in this standard, for the given e-NAND type (See Chapter 3.3.5).
The SEND_OP_COND (CMD1) command is designed to provide e-NAND hosts with a mechanism to identify and reject e-NAND which do not match the Vccq range desired by the host. This is accomplished by the host sending the required Vccq voltage window as the operand of this command (See Chapter 3.4.1). If the e-NAND can not perform data transfer in the specified range it must discard itself from further bus operations and go into Inactive State. Otherwise,
the card shall respond sending back its Vccq range. For this, the levels in the OCR register shall be defined accordingly (see Chapter 3.4).

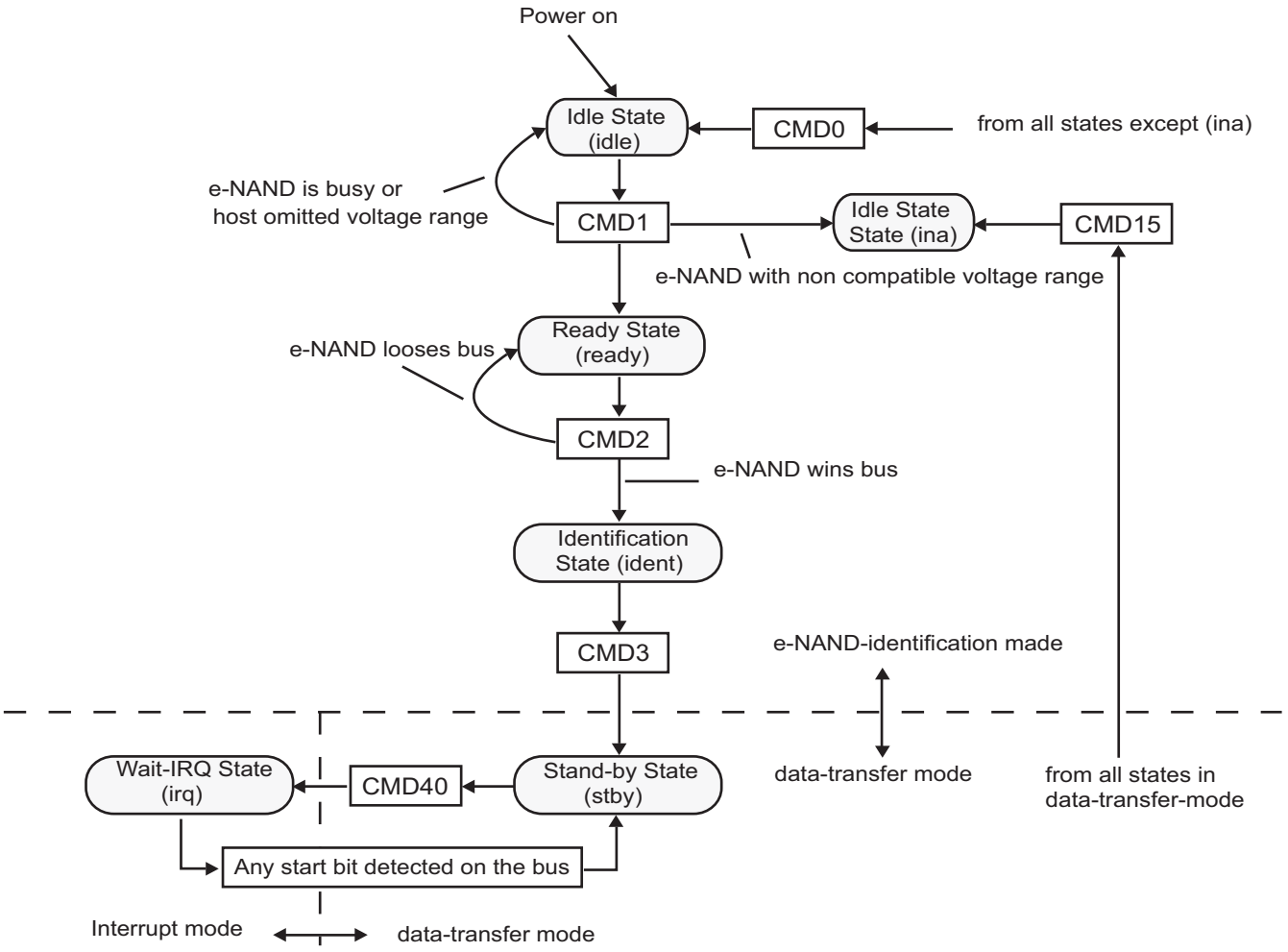


Figure 4-5 : e-NAND State Diagram (e-NAND Identification Mode)

The busy bit in the CMD1 response can be used by a e-NAND to tell the host that it is still working on its power-up/ reset procedure (e.g. downloading the register information from memory field) and is not ready yet for communication. In this case the host must repeat CMD1 until the busy bit is cleared.
During the initialization procedure, the host is not allowed to change the operating voltage range. Such changes shall be ignored by the e-NAND. If there is a real change in the operating conditions, the host must reset the e-NAND (using CMD0) and restart the initialization procedure. However, for accessing e-NAND already in Inactive State, a hard reset must be done by switching the power supply off and back on.
The command GO_INACTIVE_STATE (CMD15) can be used to send an addressed e-NAND into the Inactive State. This command is used when the host explicitly wants to deactivate a e-NAND (e.g. host is changing Vccq into a range which is known to be not supported by this e-NAND). The command CMD1 shall be implemented by all cards defined by this standard.

4.2.3 e-NAND Identification Process

The following explanation refers to a e-NAND working in a multi-card environment, as defined in versions of this standard previous to v4.0, and it is maintained for backwards compatibility to those systems.
The host starts the e-NAND identification process in open-drain mode with the identification clock rate fOD (see Chapter 3.3.10). The open drain driver stages on the CMD line allow parallel e-NAND operation during e-NAND identification. After the bus is activated, the host will request the e-NAND to send its valid operation conditions (CMD1). The response to CMD1 is the 'wired and' operation on the condition restrictions of all e-NANDs in the system. Incompatible e-NANDs are sent into Inactive State. The host then issues the broadcast command ALL_SEND_CID (CMD2), asking all e-NANDs for its unique card identification (CID) number. All unidentified e-NANDs (i.e. those which are in Ready State) simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bitstream. Those e-NANDs, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods, stop sending their CID immediately and must wait for the next identification cycle (remaining in the Ready State). Since CID numbers are unique for each e-NAND, there should be only one e-NAND which successfully sends its full CID-number to the host. This e-NAND then goes into Identification State. Thereafter, the host issues CMD3 (SET_RELATIVE_ADDR) to assign to this card a relative card address (RCA), which is shorter than CID and which will be used to address the e-NAND in the future data transfer mode (typically with a higher clock rate than fOD). Once the RCA is received the e-NAND state changes to the Stand-by State, and the e-NAND does not react to further identification cycles. Furthermore, the e-NAND switches its output drivers from open-drain to push-pull.
The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 as long as it receives a response (CID) to its identification command (CMD2). If no more e-NAND responds to this command, all e-NANDs have been identified.
The timeout condition to recognize completion of the identification process is the absence of a start bit for more than NID clock cycles after sending CMD2 (see timing values in Chapter 4.13).

4.2.4 Intrrupt Mode

The interrupt mode on the MultiMediaCard system enables the master (MultiMediaCard host) to grant the transmission allowance to the slaves (card) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a card request for service. Supporting MultiMediaCard interrupt mode is an option, both for the host and the card.
The system behavior during the interrupt mode is described in the state diagram in Figure 4-6.

- The host must ensure that the card is in Stand-by State before issuing the GO_IRQ_STATE (CMD40) command.

While waiting for an interrupt response from the card, the host must keep the clock signal active. Clock rate may be changed according to the required response time.

- The host sets the card into interrupt mode using GO_IRQ_STATE (CMD40) command.
- A card in Wait-IRQ-State is waiting for an internal interrupt trigger event. Once the event occurs, the card starts to send its response to the host. This response is sent in the open-drain mode.
- While waiting for the internal interrupt event, the card is also waiting for a start bit on the command line. Upon detection of a start bit, the card will abort interrupt mode and switch to the stand-by state.
- Regardless of winning or losing bus control during CMD40 response, the cards switches to stand-by state (as opposed to CMD2).
- After the interrupt response was received by the host, the host returns to the standard data communication procedure.

4.3 Data Transfer Mode

When the e-NAND is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. Until the contents of the CSD register is known by the host, the fPP clock rate must remain at fOD (see Chapter 3.3.10). The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, e-NAND storage capacity, maximum clock rate, etc.

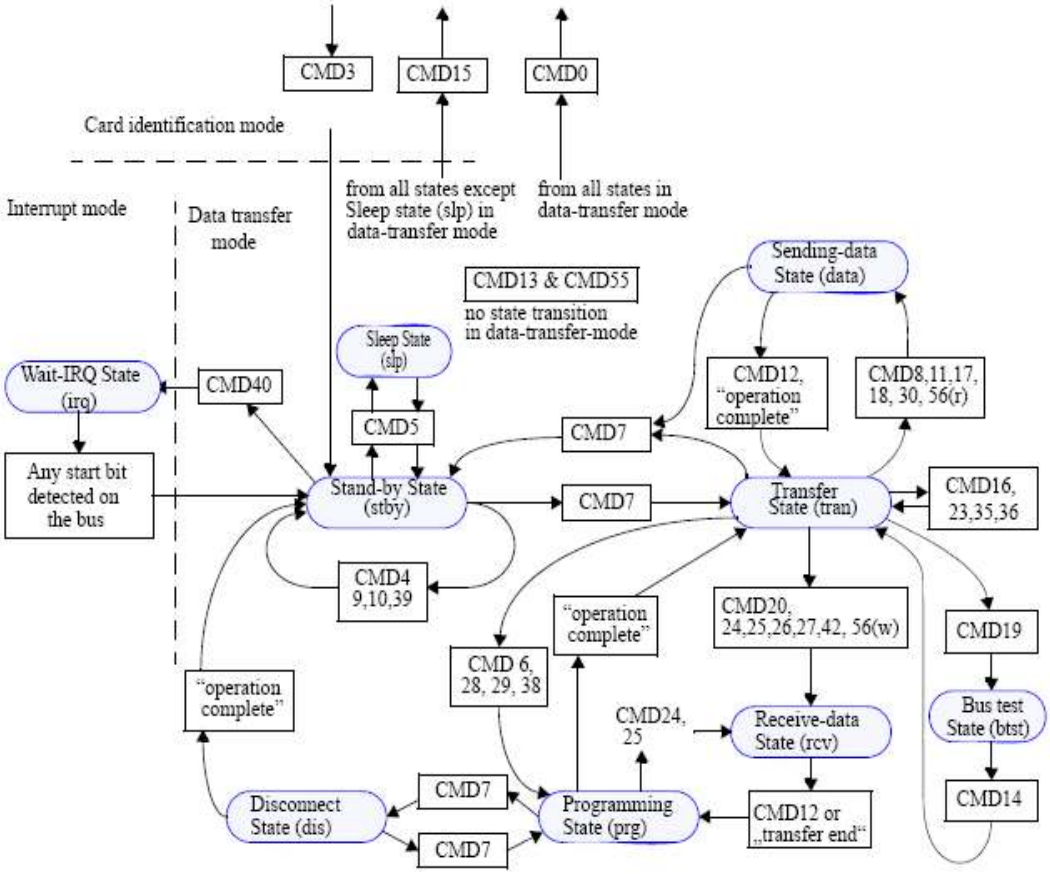


Figure 4-6 : e-NAND State Diagram (Data Transfer Mode)

The broadcast command SET_DSR (CMD4) configures the driver stages of the e-NAND. It programs its DSR register corresponding to the application bus layout (length) and the data transfer frequency. The clock rate is also switched from fOD to fPP at that point.

CMD7 is used to select the e-NAND and put it into the Transfer State. If the e-NAND was previously selected and was in Transfer State its connection with the host is released and it will move back to the Stand-by State. When CMD7 is issued with the reserved relative e-NAND address "0x0000", the e-NAND is put back to Stand-by State. After the e-NAND is assigned an RCA it will not respond to identification commands (CMD1, CMD2, CMD3, see Chapter 4.2.3).

All data communication in the Data Transfer Mode is point-to point between the host and the selected e-NAND (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.
The relationship between the various data transfer modes is summarized below (see Figure 4-6):

- All data read commands can be aborted any time by the stop command (CMD12). The data transfer will terminate and the e-NAND will return to the Transfer State. The read commands are: block read (CMD17), multiple block read (CMD18) and send write protect (CMD30).
- All data write commands can be aborted any time by the stop command (CMD12). The write commands must be stopped prior to deselecting the e-NAND by CMD7. The write commands are: block write (CMD24 and CMD25), write CID (CMD26), and write CSD (CMD27).
- As soon as the data transfer is completed, the e-NAND will exit the data write state and move either to the Programming State (transfer is successful) or Transfer State (transfer failed).
- If a block write operation is stopped and the block length and CRC of the last block are valid, the data will be programmed.
- The e-NAND may provide buffering for stream and block write. This means that the next block can be sent to the e-NAND while the previous is being programmed.
- If all write buffers are full, and as long as the card is in Programming State (see e-NAND state diagram Figure -2), the DAT0 line will be kept low.
- There is no buffering option for write CSD, write CID, write protection and erase. This means that while the e-NAND is busy servicing any one of these commands, no other data transfer commands will be accepted. DAT0 line will be kept low as long as the e-NAND is busy and in the Programming State.
- Parameter set commands are not allowed while e-NAND is programming.
  Parameter set commands are: set block length (CMD16), and erase group selection (CMD35-36).
- Read commands are not allowed while e-NAND is programming.
- Moving another e-NAND from Stand-by to Transfer State (using CMD7) will not terminate a programming opeation. The e-NAND will switch to the Disconnect State and will release the DAT0 line.
- A card can be reselected while in the Disconnect State, using CMD7. In this case the e-NAND will move to the Programming State and reactivate the busy indication.
- Resetting a e-NAND (using CMD0 or CMD15) will terminate any pending or active programming operation. This may destroy the data contents on the e-NAND. It is up to the hosts responsibility to prevent this.
- Prior to executing the bus testing procedure (CMD19, CMD14), it is recommended to set up the clock frequency used for data transfer. This way the bus test gives a true result, which might not be the case if the bus testing procedure is performed with lower clock frequency than the data transfer frequency.

In the following format definitions, all upper case flags and parameters are defined in the CSD (Chapter 3.4.3), and the other status flags in the e-NAND Status (Chapter 4.11).

4.3.1 Command Sets And Extended Settings

The e-NAND operates in a given command set, by default, after a power cycle or reset by CMD0, it is the MMC card standard command set, using a single data line, DAT0. The host can change the active command set by issuing the SWITCH command (CMD6) with the 'Command Set' access mode selected.
The supported command sets, as well as the currently selected command set, are defined in the EXT_CSD register. The EXT_CSD register is divided in two segments, a Properties segment and a Modes segment. The Properties segment contains information about the e-NAND capabilities. The Modes segment reflects the current selected modes of the e-NAND.
The host reads the EXT_CSD register by issuing the SEND_EXT_CSD command. The card sends the EXT_CSD register as a block of data, 512 bytes long. Any reserved, or write only field, reads as '0'.
The host can write the Modes segment of the EXT_CSD register by issuing a SWITCH command and setting one of the access modes. All three modes access and modify one of the EXT_CSD bytes, the byte pointed by the Index field[1]

Access Bits	Access Name	Operation
00	Command Set	The command set is changed according to the Cmd Set field of the argument
01	Set Bits	The bits in the pointed byte are set, according to the '1' bits in the Value field.
10	Clear Bits	The bits in the pointed byte are cleared, according to the '1' bits in the Value field.
11	Write Byte	The Value field is written into the pointed byte.

Table 4-1 : EXT_CSD Access Modes

The SWITCH command can be used either to write the EXT_CSD register or to change the command set. If the SWITCH command is used to change the command set, the Index and Value field are ignored, and the EXT_CSD is not written. If the SWITCH command is used to write the EXT_CSD register, the Cmd Set field is ignored, and the command set remains unchanged.
The SWITCH command response is of type R1b, therefore, the host should read the e-NAND status, using SEND_STATUS command, after the busy signal is de-asserted, to check the result of the SWITCH operation.

4.3.2 High Speed Mode Selection

After the host verifies that the e-NAND complies with version 4.0, or higher, of this standard, it has to enable the high speed mode timing in the e-NAND, before changing the clock frequency to a frequency higher than 20MHz.
After power-on, or software reset, the interface timing of the e-NAND is set as specified in Table 3-7, Chapter 5. For the host to change to a higher clock frequency, it has to enable the high speed interface timing. The host uses the SWITCH command to write 0x01 to the HS_TIMING byte, in the Modes segment of the EXT_CSD register.
The valid values for this register are defined in 'HS_TIMING', in page 37. If the host tries to write an invalid value, the HS_TIMING byte is not changed, the high speed interface timing is not enabled, and the SWITCH_ERROR bit is set.

4.3.3 Power Class Selection

After the host verifies that the e-NAND complies with version 4.0, or higher, of this standard, it may change the power class of the e-NAND.

After power-on, or software reset, the e-NAND power class is class 0, which is the default, minimum current consumption class for the card type, either High Voltage e-NAND. The PWR_CL_ff_vvv bytes, in the EXT_CSD register, reflect the power consumption levels of the e-NAND, for a 4 bits bus, an 8 bit bus, at the supported clock frequencies (26MHZ or 52MHz).

The host reads this information, using the SEND_EXT_CSD command, and determines if it will allow the e-NAND to use a higher power class. If a power class change is needed, the host uses the SWITCH command to write the POWER_CLASS byte, in the Modes segment of the EXT_CSD register.

The valid values for this register are defined in 'PWR_CL_ff_vvv', in page 84 If the host tries to write an invalid value, the POWER_CLASS byte is not changed and the SWITCH_ERROR bit is set.

4.3.4 Bus Testing Procedure

By issuing commands CMD19 and CMD14 the host can detect the functional pins on the bus. In a first step, the host sends CMD19 to the e-NAND, followed by a specific data pattern on each selected data lines. The data pattern to be sent per data line is defined in the table below. As a second step, the host sends CMD14 to request the e-NAND to send back the reversed data pattern. With the data pattern sent by the host and with the reversed pattern sent back by the e-NAND, the functional pins on the bus can be detected.

Start Bit	Data Pattern	End bit
0	1 0 x x x x ... x x	1

The e-NAND ignores all but the two first bits of the data pattern. Therefore, the e-NAND buffer size is not limiting the maximum length of the data pattern. The minimum length of the data pattern is two bytes, of which the first two bits of each data line are sent back, by the e-NAND, reversed. The data pattern sent by the host may optionally include a CRC16 checksum, which is ignored by the e-NAND.

The e-NAND detects the start bit on DAT0 and synchronizes accordingly the reading of all its data inputs.

The host ignores all but the two first bits of the reverse data pattern. The length of the reverse data pattern is eight bytes and is always sent using all the e-NAND's DAT lines (See Table through Table). The reverse data pattern sent by the e-NAND may optionally include a CRC16 checksum, which is ignored by the host.

The e-NAND has pull ups in all data inputs. In cases where the card is connected to only 1bit or only 4bit HS-MMC system, the input value of the upper bits (e.g. DAT1-DAT7 or DAT4-DAT7) are detected as logical "1" by the e-NAND.

Data line	Data pattern sent by the host	Reversed pattern sent by the e-NAND	Notes
DAT0	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	Start bit defines beginning of pattern
DAT1		0,01000000,[CRC16],1	No data pattern sent
DAT2		0,01000000,[CRC16],1	No data pattern sent
DAT3		0,01000000,[CRC16],1	No data pattern sent
DAT4		0,01000000,[CRC16],1	No data pattern sent
DAT5		0,01000000,[CRC16],1	No data pattern sent
DAT6		0,01000000,[CRC16],1	No data pattern sent
DAT7		0,01000000,[CRC16],1	No data pattern sent

Table 4-2 : 1-bit Bus Testing Pattern

Data line	Data pattern sent by the host	Reversed pattern sent by the e-NAND	Notes
DAT0	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	Start bit defines beginning of pattern
DAT1	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT2	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT3	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT4		0,01000000,[CRC16],1	No data pattern sent
DAT5		0,01000000,[CRC16],1	No data pattern sent
DAT6		0,01000000,[CRC16],1	No data pattern sent
DAT7		0,01000000,[CRC16],1	No data pattern sent

Table 4-3: 4-bit Bus Testing Pattern

Data line	Data pattern sent by the host	Reversed pattern sent by the e-NAND	Notes
DAT0	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	Start bit defines beginning of pattern
DAT1	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT2	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT3	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT4	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT5	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT6	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	
DAT7	0,10xxxxxxxxx,[CRC16],1	0,01000000,[CRC16],1	

Table 4-4 : 8-bit Bus Testing Pattern

4.3.5 Bus Width Selection

After the host has verified the functional pins on the bus it should change the bus width configuration accordingly, using the SWITCH command.

The bus width configuration is changed by writing to the BUS_WIDTH byte in the Modes Segment of the EXT_CSD register (using the SWITCH command to do so). After power-on, or software reset, the contents of the BUS_WIDTH byte is 0x00.

The valid values for this register are defined in 'BUS_WIDTH', in page 45. If the host tries to write an invalid value, the BUS_WIDTH byte is not changed and the SWITCH_ERROR bit is set. This register is write only.

4.3.6 Data Read

The DAT0-DAT7 bus line levels are high when no data is transmitted. A transmitted data block consists of a start bit (LOW), on each DAT line, followed by a continuous data stream. The data stream contains the payload data (and error correction bits if an off-card ECC is used). The data stream ends with an end bit (HIGH), on each DAT line (see Figure 4-12 - Figure 4-14). The data transmission is synchronous to the clock signal.
The payload for block oriented data transfer is protected by a CRC check sum, on each DAT line (see Chapter 6.4).

- **Block Read**

Block read is similar to stream read, except the basic unit of data transfer is a block whose maximum size is defined in the CSD (READ_BL_LEN). If READ_BL_PARTIAL is set, smaller blocks whose starting and ending address are entirely contained
within one physical block (as defined by READ_BL_LEN) may also be transmitted. Unlike stream read, a CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the *Transfer State*.
CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Two types of multiple block read transactions are defined (the host can use either one at any time):

- Open-ended Multiple block read
  The number of blocks for the read multiple block operation is not defined. The e-NAND will continuously transfer data blocks until a stop transmission command is received.

- Multiple block read with pre-defined block count
  The e-NAND will transfer the requested number of data blocks, terminate the transaction and return to *transfer* state. Stop command is not required at the end of this type of multiple block read, unless terminated with an error. In order to start a multiple block read with pre-defined block count the host must use the SET_BLOCK_COUNT command (CMD23) immediately preceding the READ_MULTIPLE_BLOCK (CMD18) command. Otherwise the e-NAND will start an open -ended multiple block read which can be stopped using the STOP_TRANSMISION command.

The host can abort reading at any time, within a multiple block operation, regardless of the its type. Transaction abort is done by sending the stop transmission command.

If either one of the following conditions occur, the e-NAND will reject the command, remain in *Tran* state and respond with the respective error bit set.

- The host provides an out of range address as an argument to either CMD17 or CMD18. ADDRESS_OUT_OF_RANGE is set.
- The currently defined block length is illegal for a read operation. BLOCK_LEN_ERROR is set.
- The address/block-length combination positions the first data block misaligned to the card physical blocks. ADDRESS_MISALIGN is set.

If the e-NAND detects an error (e.g. out of range, address misalignment, internal error, etc.) during a multiple block read operation (both types) it will stop data transmission and remain in the Data State. The host must then abort the operation by sending the stop transmission command. The read error is reported in the response to the stop transmission command.

If the host sends a stop transmission command after the e-NAND transmits the last block of a multiple block operation with a pre-defined number of blocks, it is regarded as an illegal command, since the e-NAND is no longer in data state.

If the host uses partial blocks whose accumulated length is not block aligned, and block misalignment is not allowed, the e-NAND shall detect a block misalignment error condition during the transmission of the first misaligned block and the content of the further transferred bits is undefined. As the host sends CMD12 the card will respond with the ADDRESS_MISALIGN bit set and return to Tran state.

If the host sets the argument of the SET_BLOCK_COUNT command (CMD23) to all 0s, then the command is accepted; however, a subsequent read will follow the open-ended multiple block read protocol (STOP_TRANSMISSION command - CMD12 - is required).

If a host had sent a CMD16 for password setting to a higher than 2GB of density of card, then this host MUST re-send CMD16 before read data transfer; otherwise, the card will response a BLK_LEN_ERROR and stay in TRANS state without data transfer since the data block (except in password application) trans fer is sector unit (512B). Same error applies to up to 2GB of density of cards in case partial read access are not supported.

4.3.7 Data Write

The data transfer format of write operation is similar to the data read. For block oriented write data transfer, the CRC check bits are added to each data block. The e-NAND performs a CRC parity check (see Chapter 6.4) for each received data block prior to the write operation. By this mechanism, writing of erroneously transferred data can be prevented.

- **Block Write**

During block write (CMD24 - 27) one or more blocks of data are transferred from the host to the e-NAND with a CRC appended to the end of each block by the host. A e-NAND supporting block write shall always be able to accept a block of data defined by WRITE_BL_LEN. If the CRC fails, the e-NAND shall indicate the failure on the DAT0 line (see below); the transferred data will be discarded and not written, and all further transmitted blocks (in multiple block write mode) will be ignored.

CMD25 (WRITE_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Two types of multiple block write transactions, identical to the multiple block read, are defined (the host can use either one at any time):

- Open-ended Multiple block write

  The number of blocks for the write multiple block operation is not defined. The e-NAND will continuously accept and program data blocks until a stop transmission command is received.

- Multiple block write with pre-defined block count

  The e-NAND will accept the requested number of data blocks, terminate the transaction and return to transfer state.

  Stop command is not required at the end of this type of multiple block write, unless terminated with an error. In order to start a multiple block write with pre-defined block count the host must use the SET_BLOCK_COUNT com mand (CMD23) immediately preceding the WRITE_MULTIPLE_BLOCK (CMD25) command. Otherwise the e-NAND will start an open -ended multiple block write which can be stopped using the STOP_TRANSMISION command.

- Reliable Write: Multiple block write with pre-defined block count and Reliable Write parame ters.

This transaction is similar to the basic pre-defined multiple-block write (defined in previous bullet) with the following exceptions. The old data pointed to by a logical address must remain unchanged as long as the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. Data must remain valid even if a sudden power loss occurs during the programming. A maximum of two different sizes of reliable write transactions are supported: 512B and the Reliable Write Sector Count parameter in EXT_CSD (REL_WR_SEC_C) multiplied by 512B. The function is activated by setting the Reliable Write Request parameter (bit 31) to "1" in the SET_BLOCK_COUNT command (CMD23) argument. The Reliable Write Sector Count parameter in EXT_CSD indicates the supported write sector count. The reliable write function is only possible under the following conditions: the length of the write operation equals the supported reliable write size or 512B, AND the reliable write request is active. Otherwise the transaction is handled as basic pre-defined multiple block case. When the length of the write operation is set to "0," the operation is executed as a basic, openended, multiple-blockwrite case, even when the reliable write request is active.

The host can abort writing at any time, within a multiple block operation, regardless of the its type. Transaction abort is done by sending the stop transmission command. If a multiple block write with pre-defined block count is aborted, the data in the remaining blocks is not defined.

If either one of the following conditions occur, the e-NAND will reject the command, remain in Tran state and respond with the respective error bit set.

- The host provides an out of range address as an argument to either CMD24 or CMD25. ADDRESS_OUT_OF_RANGE is set.
- The currently defined block length is illegal for a write operation. BLOCK_LEN_ERROR is set.
- The address/block-length combination positions the first data block misaligned to the e-NAND physical blocks. ADDRESS_MISALIGN is set.

If the e-NAND detects an error (e.g. write protect violation, out of range, address misalignment, internal error, etc.) during a multiple block write operation (both types) it will ignore any further incoming data blocks and remain in the Receive State.

The host must then abort the operation by sending the stop transmission command. The write error is reported in the response to the stop transmission command.

If the host sends a stop transmission command after the e-NAND received the last data block of a multiple block write with a pre-defined number of blocks, it is regarded as an illegal command, since the e-NAND is no longer in data state.

If the host uses partial blocks whose accumulated length is not block aligned, and block misalignment is not allowed (CSD parameter WRITE_BLK_MISALIGN is not set), the e-NAND shall detect the block misalignment error during the reception of the first misaligned block, abort the write operation, and ignore all further incoming data. As the host sends CMD12, the e-NAND will respond with the ADDRESS_MISALIGN bit set and return to Tran state.

If the host sets the argument of the SET_BLOCK_COUNT command (CMD23) to all 0s, then the command is accepted; however, a subsequent write will follow the open-ended multiple block write protocol (STOP_TRANSMISSION command - CMD12 - is required).

Programming of the CID and CSD registers does not require a previous block length setting. The transferred data is also CRC protected. If a part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents.

e-NAND may require long and unpredictable times to write a block of data. After receiving a block of data and completing the CRC check, the e-NAND will begin writing and hold the DAT0 line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the e-NAND with a SEND_STATUS command (CMD13) at any time, and the e-NAND will respond with its status. The status bit READY_FOR_DATA indicates whether the e-NAND can accept new data or whether the write process is still in progress). The host may deselect the e-NAND by issuing CMD7 which will displace the e-NAND into the Disconnect State and release the DAT0 line without interrupting the write operation.

When reselecting the e-NAND, it will reactivate busy indication by pulling DAT0 to low if programming is still in progress and the write buffer is unavailable.

4.3.8 CSD Programming

Programming of the CSD register does not require a previous block length setting. After sending CMD27 and receiving an R1 response, the start bit (=0)is sent, the modified CSD register (=16 bytes), CRC16 (=2bytes), and end bit (=1). The host can change only the least significant 16bits [15:0] of the CSD. The rest of the CSD register content must match the e-NAND CSD Register. If the e-NAND detects a content inconsistency between the old and new CSD register, it will not reprogram the CSD in order to ensure validity of the CRC field in the CSD register.
Bits [7:1] are the CRC7 of bits [127:8] of the CSD register, which should be recalculated once the register changes. After calculating CRC7, the CRC16 should also be calculated for all of the CSD register [127:0].

4.3.9 Erase

e-NAND, in addition to the implicit erase executed by the e-NAND as part of the write operation, provides a host explicit erase function. The erasable unit of the e-NAND is the "Erase Group"; Erase group is measured in write blocks which are the basic writable units of the e-NAND. The size of the Erase Group is a e-NAND specific parameter and defined in the CSD. The content of an explicitly erased memory range shall be 0.
The host can erase a contiguous range of Erase Groups. Starting the erase process is a three steps sequence. First the host defines the start address of the range using the ERASE_GROUP_START (CMD35) command, next it defines the last address of the range using the ERASE_GROUP_END (CMD36) command and finally it starts the erase process by issuing the ERASE (CMD38) command. The address field in the erase commands is an Erase Group address in byte units. The e-NAND will ignore all LSB's below the Erase Group size, effectively rounding the address down to the Erase Group boundary.

If an erase command (either CMD35, CMD36, CMD38) is received out of the defined erase sequence, the e-NAND shall set the ERASE_SEQ_ERROR bit in the status register and reset the whole sequence.
If the host provides an out of range address as an argument to CMD35 or CMD36, the e-NAND will reject the command, respond with the ADDRESS_OUT_OF_RANGE bit set and reset the whole erase sequence.
If an 'non erase' command (neither of CMD35, CMD36, CMD38 or CMD13) is received, the e-NAND shall respond with the ERASE_RESET bit set, reset the erase sequence and execute the last command. Commands not addressed to the selected e-NAND do not abort the erase sequence.
If the erase range includes write protected blocks, they shall be left intact and only the non protected blocks shall be erased. The WP_ERASE_SKIP status bit in the status register shall be set.
As described above for block write, the e-NAND will indicate that an erase is in progress by holding DAT0 low. The actual erase time may be quite long, and the host may issue CMD7 to deselect the e-NAND.

4.3.10 Write Protect Management

In order to allow the host to protect data against erase or write, the e-NAND shall support two levels of write protect commands:

- The entire e-NAND may be write protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of the e-NAND may be write protected. The segment size is defined in units of WP_GRP_SIZE erase groups as specified in the CSD. The SET_WRITE_PROT command sets the write protection of the addre write-pro tect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.

The SEND_WRITE_PROT command is similar to a single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits.
The address field in the write protect commands is a group address in byte units. The card will ignore all LSBs below the group size.
If the host provides an out of range address as an argument to CMD28, CMD29 or CMD30, the card will reject the command, respond with the ADDRESS_OUT_OF_RANGE bit set and remain in the Tran state.

4.3.11 Card Lock/Unlock Operation

The password protection feature enables the host to lock the e-NAND by providing a password, which later will be used for unlocking the e-NAND. The password and its size is kept in an 128 bit PWD and 8 bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.

A locked e-NAND responds to (and executes) all commands in the "basic" command class (class 0) and "lock e-NAND" command class. Thus the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the e-NAND. If the password was previously set (the value of PWD_LEN is not '0') the e-NAND will be locked automatically after power on.

Similar to the existing CSD and CID register write commands the lock/unlock command is available in "transfer state" only.

This means that it does not include an address argument and the e-NAND has to be selected before using it.

The e-NAND lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). The following table describes the structure of the command data block.

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved				ERASE	LOCK_UNLOCK	CLR_PWD	SET_PWD
1	PWD_LEN							
2	Password data							
...								
PWD_LEN + 1								

Table 4-5 : Lock Card Data Structure

- **ERASE:** 1 Defines Forced Erase Operation (all other bits shall be 0) and only the cmd byte is sent.
- **LOCK/UNLOCK**: 1 = Locks the e-NAND. 0 = Unlock the e-NAND (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).
- **CLR_PWD**: 1 = Clears PWD.
- **SET_PWD**: 1 = Set new password to PWD
- **PWD_LEN**: Defines the following password length (in bytes). Valid password length are 1 to 16 bytes.
- **PWD:** The password (new or currently used depending on the command).

The data block size shall be defined by the host before it sends the e-NAND lock/unlock command. This will allow different password sizes.

The following paragraphs define the various lock/unlock command sequences:

- **Setting the Password**
  - Select the 7D (CMD7), if not previously selected already

- Define the block length (CMD16), given by the 8bit e-NAND lock/unlock mode, the 8 bits password size (in bytes), and the number of bytes of the new password. In case that a password *replacement* is done, then the block size shall consider that both passwords, the old and the new one, are sent with the command.
- Send e-NAND Lock/Unlock command with the appropriate data block size on the data line including 16 bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWD_LEN) and the password itself. In case that a password *replacement* is done, then the length value (PWD_LEN) shall include both passwords, the old and the new one, and the PWD field shall include the old password (currently used) followed by the new pass word.
- In case that a password replacement is attempted with PWD_LEN set to the length of the old pass-word only, the LOCK_UNLOCK_FAILED error bit is set in the status register and the old password is not changed.
- In case that the sent old password is not correct (not equal in size and content) then LOCK_UNLOCK_ FAILED error bit will be set in the status register and the old password does not change.
  In case that PWD matches the sent old password then the given new password and its size will be saved in the PWD and PWD_LEN fields, respectively.

Note that the password length register (PWD_LEN) indicates if a password is currently set. When it equals '0' there is no password set. If the value of PWD_LEN is not equal to zero the e-NAND will lock itself after power up. It is possible to lock the e-NAND immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the pass-word) or sending additional command for card lock.

- **Reset the Password:**

  - Select the card (CMD7), if not previously selected already
  - Define the block length (CMD16), given by the 8 bit e-NAND lock/unlock mode, the 8 bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the e-NAND lock/unlock command with the appropriate data block size on the data line including 16 bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWD_LEN) and the password (PWD) itself (LOCK/ UNLOCK bit is dont care). If the PWD and PWD_LEN content match the sent password and its size, then the con tent of the PWD register is cleared and PWD_LEN is set to 0. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

- **Locking a e-NAND:**

  - Select the e-NAND (CMD7), if not previously selected already
  - Define the block length (CMD16), given by the 8 bit e-NAND lock/unlock mode, the 8 bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the card lock/unlock command with the appropriate data block size on the data line including 16 bit CRC. The data block shall indicate the mode LOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the e-NAND will be locked and the e-NAND-locked status bit will be set in the status register. If the password is not correct then LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that it is possible to set the password and to lock the e-NAND in the same sequence. In such case the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent.
If the password was previously set (PWD_LEN is not '0'), then the e-NAND will be locked automatically after power on reset. An attempt to lock a locked e-NAND or to lock a e-NAND that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register.

- **Unlocking the card:**

  - Select the e-NAND (CMD7), if not previously selected already.
  - Define the block length (CMD16), given by the 8 bit e-NAND lock/unlock mode, the 8 bit password size (in bytes), and the number of bytes of the currently used password.
  - Send the e-NAND lock/unlock command with the appropriate data block size on the data line including 16 bit CRC. The data block shall indicate the mode UNLOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the e-NAND will be unlocked and the e-NAND-locked status bit will be cleared in the status register. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that the unlocking is done only for the current power session. As long as the PWD is not cleared the e-NAND will be locked automatically on the next power up. The only way to unlock the e-NAND is by clearing the password.
An attempt to unlock an unlocked e-NAND will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

- **Forcing Erase:**

In case that the user forgot the password (the PWD content) it is possible to erase all the e-NAND data content along with the PWD content. This operation is called *Forced Erase*.

  - Select the e-NAND (CMD7), if not previously selected already.
  - Define the block length (CMD16) to 1 byte (8bit card lock/unlock command). Send the e-NAND lock/unlock command with the appropriate data block of one byte on the data line including 16 bit CRC. The data block shall indicate the mode ERASE (the ERASE bit shall be the only bit set).

If the ERASE bit is not the only bit in the data field then the LOCK_UNLOCK_FAILED error bit will be set in the status register and the erase request is rejected.
If the command was accepted then ALL THE e-NAND CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked e-NAND will get unlocked. In addition, if the e-NAND is temporary write protected it will be unprotected (write enabled), the temporary-write-protect bit in the CSD and all Write-Protect-Groups will be cleared. An attempt to force erase on an unlocked e-NAND will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register. If a force erase command is issued on a permanently-write-protect media the command will fail (e-NAND stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register.
The Force Erase time-out is specified in Chapter 4.6.2

7.3.12 Sleep (CMD5)

A card may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. In this state the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. The timeout for state transitions between Standby state and Sleep state is defined in the EXT_CSD register S_A_timeout. The maximum current consumptions during the Sleep state are defined in the EXT_CSD registers S_A_VCC and S_A_VCCQ.

Sleep command: The bit 15 as set to 1 in SLEEP/AWAKE (CMD5) argument.

Awake command: The bit 15 as set to 0 in SLEEP/AWAKE (CMD5) argument.

The Sleep command is used to initiate the state transition from Standby state to Sleep state. The memory device indicates the transition phase busy by pulling down the DAT0 line. No further commands should be sent during the busy. The Sleep state is reached when the memory device stops pulling down the DAT0 line.
The Awake command is used to initiate the transition from Sleep state to Standby state. The memory device indicates the transition phase busy by pulling down the DAT0 line. No further commands should be sent during the busy. The Standby state is reached when the memory device stops pulling down the DAT0 line.
During the Sleep state the Vcc power supply may be switched off. This is to enable even further system power consumption saving. The Vcc supply is allowed to be switched off only after the Sleep state has been reached (the memory device has stopped to pull down the DAT0 line). The Vcc supply have to be ramped back up at least to the min operating voltage level before the state transition from Sleep state toStandby state is allowed to be initiated (Awake command).

4.4 Clock Control

The e-NAND bus clock signal can be used by the host to put the e-NAND into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down.
There are a few restrictions the host must follow:

- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency, defined by the e-NAND, and the identification frequency defined by the specification document).
- It is an obvious requirement that the clock must be running for the e-NAND to output data or response tokens. Afte the last e-NAND bus transaction, the host is required, to provide **8 (eight)** clock cycles for the e-NAND to complete the operation before shutting down the clock. Following is a list of the various bus transactions:
- A command with no response. 8 clocks after the host command end bit.
- A command with response. 8 clocks after the card response end bit.
- A read data transaction. 8 clocks after the end bit of the last data block.
- A write data transaction. 8 clocks after the CRC status token.
- The host is allowed to shut down the clock of a busy e-NAND. The card will complete the programming operation regardless of the host clock. However, the host must provide a clock edge for the e-NAND to turn off its busy signal. Without a clock edge the e-NAND (unless previously disconnected by a deselect command -CMD7) will force the DAT0 line down, forever.

4.5 Cyclic Redundancy Codes (CRC)

The CRC is intended for protecting e-NAND commands, responses and data transfer against transmission errors on the e-NAND bus. One CRC is generated for every command and checked for every response on the CMD line.
For data blocks one CRC per transferred block, per data line, is generated. The CRC is generated and checked as described in the following.

- **CRC7**

The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:

Generator polynomial $G(x) = x^7 + x^3 + 1$

$M(x) = (\text{first bit}) \times x^n + (\text{second bit}) \times x^{n-1} + \ldots + (\text{last bit}) \times x^0$

$CRC[6...0] = \text{Remainder}[(M(x) \cdot x^7) / G(x)]$

All CRC registers are initialized to zero. The first bit is the most left bit of the corresponding bit string (of the command, response, CID or CSD). The degree *n* of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

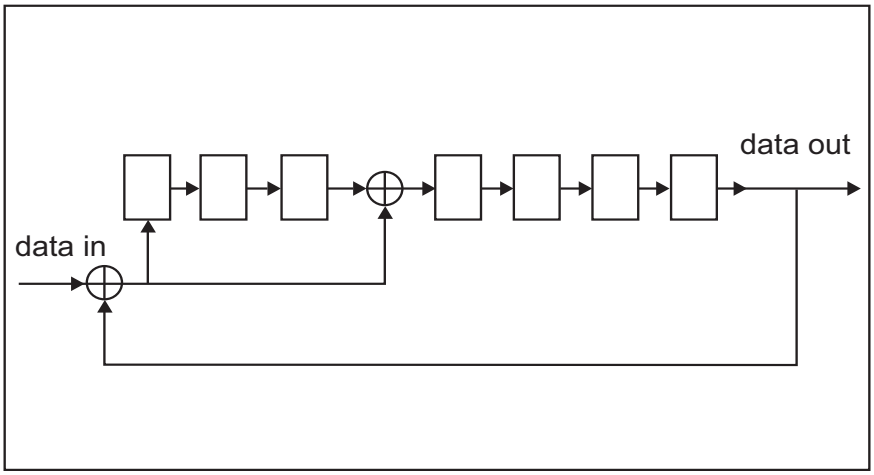


Figure 4-7 : CRC7 Generator/Checker

● **CRC16**

The CRC16 is used for payload protection in block transfer mode. The CRC check sum is a 16-bit value and is computed as follows:

Generator polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$

$M(x) = (\text{first bit}) \times x^n + (\text{second bit}) \times x^{n-1} + \ldots + (\text{last bit}) \times x^0$

$CRC[15...0] = \text{Remainder}[(M(x) \cdot x^{16}) / G(x)]$

All CRC registers are initialized to zero. The first bit is the first data bit of the corresponding block. The degree *n* of the polynomial denotes the number of bits of the data block decreased by one (e.g. n = 4095 for a block length of 512 bytes).

The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2048 Bytes (n <= 16383).

The same CRC16 calculation is used for all bus configurations. In 4 bit and 8 bit bus configurations, the CRC16 is calculated for each line separately. Sending the CRC is synchronized so the CRC code is transferred at the same time in all lines.

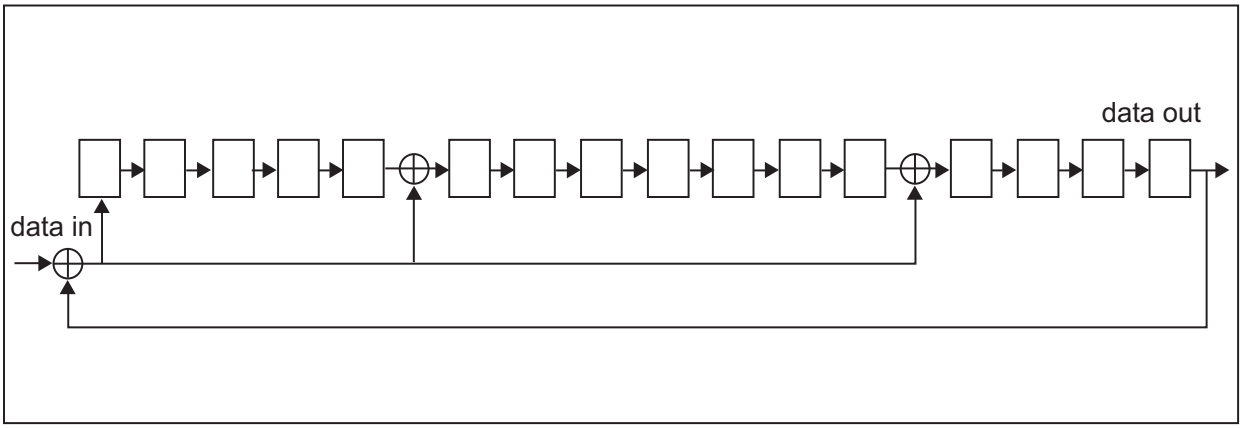


Figure 4-8 : CRC16 Generator/Checker

4.6 Error Conditions

4.6.1 CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed e-NAND's CRC check fails, the e-NAND does not respond, and the command is not executed; the e-NAND does not change its state, and COM_CRC_ERROR bit is set in the status register.
Similarly, if an illegal command has been received, the e-NAND shall not change its state, shall not respond and shall set the ILLEGAL_COMMAND error bit in the status register. Only the non-erroneous state branches are shown in the state diagrams (see Figure 4-1 to Figure 4-2). Table 4-18 contains a complete state transition description.
There are different kinds of illegal commands:

- Commands which belong to classes not supported by the e-NAND (e.g. write commands in read only e-NAND).
- Commands not allowed in the current state (e.g. CMD2 in Transfer State).
- Commands which are not defined (e.g. CMD44).

4.6.2 Read, Write, Erase And Force Erase Time-out Conditions

The times after which a time-out condition for read/write/erase operations occurs are (e-NAND independent) **10 times longer** than the typical access/program times for these operations given below. A e-NAND shall complete the command within this time period, or give up and return an error message. If the host does not get a response within the defined time-out it should assume the e-NAND is not going to respond anymore and try to recover (e.g. reset the e-NAND, power cycle, reject, etc.). The typical access and program times are defined as follows:

- **Read**

The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC (see Chapter 4.13). These e-NAND parameters define the typical delay between the end bit of the read command and the start bit of the data block.

- **Write**

The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write/erase commands (e.g. SET(CLEAR)_WRITE_PROTECT, PROGRAM_CSD(CID) and the block write commands).

- **Erase**

The duration of an erase command will be (order of magnitude) the number of write blocks to be erased multiplied by the block write delay.

- **Force Erase**

The duration of the Force Erase command using CMD42 is specified to be a fixed time-out of 3 minutes.

4.7 Minimum Performance

The e-NAND has to fullfill the requirements set for the read and write access performance.

4.7.1 Speed Class Definition

The speed class definition is for indication of the minimum performance of a e-NAND. The classes are defined based on the 150kB/s base value. The minimum performance of the e-NAND can then be marked by defined multiples of the base value e.g. 2.4MB/s. Only following speed classes are defined (note that e-NANDs are always including 8bit data bus and the categories below states the configuration with which the e-NAND is operated):

Low bus category classes (26MHz clock with 4bit data bus operation)

- 2.4 MB/s Class A
- 3.0 MB/s Class B
- 4.5 MB/s Class C
- 6.0 MB/s Class D
- 9.0 MB/s Class E

Mid bus category classes (26MHz clock with 8bit data bus or 52MHz clock with 4bit data bus operation):

- 12.0 MB/s Class F
- 15.0 MB/s Class G
- 18.0 MB/s Class H
- 21.0 MB/s Class J

High bus category classes (52MHz clock with 8bit data bus operation):

- 24.0 MB/s Class K
- 30.0 MB/s Class M
- 36.0 MB/s Class O
- 42.0 MB/s Class R
- 48.0 MB/s Class T

The performance values for both write and read accesses are stored into the EXT_CSD register for electrical reading (see chapter 3.4.5 on page 48). Only the defined values and classes are allowed to be used.

4.7.2 Absolute Minimum

Absolute minimum read and write access performance which all e-NAND has to fullfill is 2.4MB/s. This is the Class A.

4.7.3 Measurement of the Performance

The procedure for the measurement of the performance of the e-NAND is defined in detail in the Compliance Documentation.
Initial state of the memory in prior to the test is: filled with random data. The test is performed by writing/reading a 64kB chunk of data to/from random logical addresses (aligned to physical block boundaries)of the e-NAND. A predefined multiple block write/read is used with block count of 128 (64kB as 512B blocks are used). The performance is calculated as average out of several 64kB accesses.

Same test is performed with all applicable clock frequency and bus width options as follows:

- 52MHz, 8bit bus (if 52MHz clock frequency is supported by the e-NAND)
- 52MHz, 4bit bus (if 52MHz clock frequency is supported by the e-NAND)
- 26MHz, 8bit bus
- 26MHz, 4bit bus

In case the minimum performance of the e-NAND exceeds the physical limit of one of the above mentioned options the e-NAND has to also fulfill accordingly the performance criteria as defined in **MIN_PERF_a_b_ff** on page 42.

4.8 Commands

4.8.1 Command Types

There are four kinds of commands defined to control the e-NAND:

* broadcast commands (bc), no response
* broadcast commands with response (bcr)
* addressed (point-to-point) commands (ac), no data transfer on DAT lines
* addressed (point-to-point) data transfer commands (adtc), data transfer on DAT lines
* All commands and responses are sent over the CMD line of the e-NAND bus. The command transmission always starts with the left bit of the bitstring corresponding to the command codeword.

4.8.2 Command Format

All commands have a fixed code length of 48 bits, needing a transmission time of 0.92 microSec @ 52 MHz

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	command index	argument	CRC7	end bit

Table 4-6 : Format

A command always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (host = '1').
The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by 'x' in the table above indicates this variable is dependent on the command. All commands are protected by a CRC (see Chapter 4.5 for the definition of CRC7). Every command codeword is terminated by the end bit (always '1'). All commands and their arguments are listed in Table 4-7 -Table 4-17.

4.8.3 Command Classes

The command set of the e-NAND is divided into several classes (See Table 4-7). Each class supports a subset of e-NAND functions.
Class 0 is mandatory and shall be supported by all e-NANDs. The other classes are either mandatory only for specific e-NAND types or optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each e-NAND, providing the host with information on how to access the e-NAND.

Card Command Class (CCC)	Class Description	Supported commands																			
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
class 0	basic	+	+	+	+	+	+	+	+	+	+	+		+	+	+	+				+	
class 1	stream read												+									
class 2	block read																	+	+	+		
class 3	stream write																					+
class 4	block write																	+				
class 5	erase																					
class 6	write protection																					
class 7	lock card																	+				
class 8	application specific																					
class 9	I/O mode																					
class 10-11	reserved																					

Card Command Class (CCC)	Class Description	Supported commands															
		23	24	25	26	27	28	29	30	35	36	38	39	40	42	55	56
class 0	basic																
class 1	stream read																
class 2	block read	+															
class 3	stream write																
class 4	block write	+	+	+	+	+											
class 5	erase									+	+	+					
class 6	write protection						+	+	+								
class 7	lock card														+		
class 8	application specific															+	+
class 9	I/O mode												+	+			
class 10-11	reserved																

Table 4-7 : Card Command Classes (CCC)

Note: Support MMC command class :
-Class 0, 2, 4, 5, 6, 7, 8

4.8.4 Detailed Command Description

The following tables define in detail all e-NANDs bus commands. The responses R1-R5 are defined in Chapter 4.10. The registers CID, CSD, EXT_CSD and DSR are described in Chapter 3.4.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	Resets the e-NAND to idle state
CMD1	bcr	[31:0] OCR without busy	R3	SEND_OP_COND	Asks the e-NAND, in idle state, to send its Operating Conditions Register contents in the response on the CMD line.
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks the e-NAND to send its CID number on the CMD line
CMD3	ac	[31:16] RCA [15:0] stuff bits	R1	SET_RELATIVE_ADDR	SET_RELATIVE_ADDR
CMD4	ac	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of the Card
CMD5	ac	[31:16] RCA [15] Sleep/Awake [14:0] stuff bits	R1b	SLEEP_AWAKE	Toggles the card between Sleep state and Standby state. (See Section 7.3.12)
CMD6	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] Cmd Set	R1b	SWITCH	Switches the mode of operation of the selected e-NAND or modifies the EXT_CSD registers. (See chapter 4.3.1)
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1b[a]	SELECT/ DESELECT_e-NAND	Command toggles a e-NAND between the stand-by and transfer states or between the programming and disconnect states. In both cases the e-NAND is selected by its own relative address and gets deselected by any other address; address 0 deselects the e-NAND.
CMD8	adtc	[31:0] stuff bits	R1	SEND_EXT_CSD	The e-NAND sends its EXT_CSD register as a block of data.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	Addressed e-NAND sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	Addressed e-NAND sends its card identification (CID) on CMD the line.
CMD11	Not Supported				
CMD12	ac	[31:0] stuff bits	R1b	STOP_TRANSMISSION	Forces the e-NAND to stop transmission
CMD13	ac	[31:16] RCA [15:0] stuff bits	R1	SEND_STATUS	Addressed e-NAND sends its status register.
CMD14	adtc	[31:0] stuff bits	R1	BUSTEST_R	A host reads the reversed bus testing data pattern from a e-NAND.

CMD15	ac	[31:16] RCA [15:0] stuff bits	-	GO_INACTIVE_STATE	Sets the e-NAND to inactive state
CMD19	adtc	[31:0] stuff bits	R1	BUSTEST_W	A host sends the bus test data pattern to a e-NAND.

Table 4-8 : Basic Commands And Read Stream Commands (Class 0 And Class 1)

a. R1 while selecting from Stand-By State to Transfer State; R1b while selecting from Disconnected State to Programming State.
b. Data address for media =<2GB is a 32bit byte address and data address for media > 2GB is a 32bit sector (512B) address.
c. R1 for read cases and R1b for write cases.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Sets the block length (in bytes) for all following block commands (read and write). Default block length is specified in the CSD.
CMD17	adtc	[31:0] data address	R1	READ_SINGLE_BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.[a]
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	Continuously transfers data blocks from e-NAND to host until interrupted by a stop command, or the requested number of data blocks is transmitted

Table 4-9 : Block Oriented Read Commands (Class 2)

a.The transferred data must not cross a physical block boundary, unless READ_BLK_MISALIGN is set in the CSD register

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD20	ac	[31:0] data address	R1	WRITE_DAT_UNTIL_STOP	Writes a data stream from the host, starting at the given address, until a STOP_TRANSMISSION follows.
CMD21 ... CMD22	reserved				

a. Data address for media =<2GB is a 32bit byte address and data address for media > 2GB is a 32bit sector (512B) address.

Table 4-10 : Stream Write Commands (Class 3)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD23	ac	[31] Reliable Write Request [30:16] set to 0 [15:0] number of blocks	R1	SET_BLOCK_COUNT	Defines the number of blocks which are going to be transferred in the immediately succeeding multiple block read or write command. If the argument is all 0s, the subsequent read/ write operation will be open-ended.
CMD24	adtc	[31:0] data address	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.[a]
CMD25	adtc	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows or the requested number of block received.
CMD26	adtc	[31:0] stuff bits	R1	PROGRAM_CID	Programming of the card identification register. This command shall be issued only once. The card contains hardware to prevent this operation after the first programming. Normally this command is reserved for the manufacturer.
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

Table 4-11 : Block Oriented Write Commands (Class 4)

a.The transferred data must not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD28	ac	[31:0] data address	R1b	SET_WRITE_PROT	If the e-NAND has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29	ac	[31:0] data address	R1b	CLR_WRITE_PROT	If the e-NAND provides write protection features, this command clears the write protection bit of the addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	If the e-NAND provides write protection features, this command asks the e-NAND to send the status of the write protection bits. [a]
CMD31	Reserved				

Table 4-13 : Block Oriented Write Protection Commands (Class 6)

a. 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD32 ... CMD34	Reserved. These command indexes cannot be used in order to maintain backwards compatibility with older versions of the e-NAND				
CMD35	ac	[31:0] data address	R1	ERASE_GROUP_START	Sets the address of the first erase group within a range to be selected for erase
CMD36	ac	[31:0] data address	R1	ERASE_GROUP_END	Sets the address of the last erase group within a continuous range to be selected for erase
CMD37	Reserved. This command index cannot be used in order to maintain backwards compatibility with older versions of the e-NAND				
CMD38	ac	[31:0] stuff bits	R1b	ERASE	Erases all previously selected write blocks

Table 4-14 : Erase Commands (Class 5)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD39 CMD40	MMCA Optional Command, currently not supported.				
CMD41	Reserved				

Table 4-15 : I/O Mode Commands (Class 9)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD42	adtc	[31:0] stuff bits.	R1b	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the e-NAND. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43... CMD54	Reserved				

Table 4-16 : Lock e-NAND (Class 7)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD55 CMD56	MMCA Optional Command, currently not supported.				
CMD57 ... CMD59	Reserved				
CMD60 ... CMD63	Reserved for manufacturer				

Table 4-17 : Application Specific Commands (Class 8)

All future reserved commands shall have a codeword length of 48 bits, as well as their responses (if there are any).

4.9 e-NAND State Transition

Table defines the e-NAND state transitions in dependency of the received command.

	Current State												
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**btst**	**rcv**	**prg**	**dis**	**ina**	**slp**	**irq**
Command	Changes to												
Class Independent													
CRC error	-	-	-	-	-	-	-	-	-	-	-	-	stby
command not supported	-	-	-	-	-	-	-	-	-	-	-	-	stby
Class 0													
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	idle	-	idle	stby
CMD1, e-NAND Vccq range compatible	ready	-	-	-	-	-	-	-	-	-	-	-	stby
CMD1, e-NAND is busy	idle	-	-	-	-	-	-	-	-	-	-	-	stby
CMD1, e-NAND Vccq range not compatible	ina	-	-	-	-	-	-	-	-	-	-	-	stby
CMD2, e-NAND wins bus	-	ident	-	-	-	-	-	-	-	-	-	-	stby
CMD2, e-NAND loses bus	-	ready	-	-	-	-	-	-	-	-	-	-	stby
CMD3	-	-	stby	-	-	-	-	-	-	-	-	-	stby
CMD4	-	-	-	stby	-	-	-	-	-	-	-	-	stby
CMD5	-	-	-	slp	-	-	-	-	-	-	-	stby	stby
CMD6	-	-	-	-	prg	-	-	-	-	-	-	-	stby
CMD7, card is addressed	-	-	-	tran	-	-	-	-	-	prg	-	-	stby
CMD7, card is not addressed	-	-	-	-	stby	stby	-	-	dis	-	-	-	stby
CMD8	-	-	-	-	data	-	-	-	-	-	-	-	stby
CMD9	-	-	-	stby	-	-	-	-	-	-	-	-	stby
CMD10	-	-	-	stby	-	-	-	-	-	-	-	-	stby
CMD12	-	-	-	-	-	tran	-	prg	-	-	-	-	stby
CMD13	-	-	-	stby	tran	data	btst	rcv	prg	dis	-	-	stby
CMD14	-	-	-	-	-	-	tran	-	-	-	-	-	stby
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	ina	-	-	stby
CMD19	-	-	-	-	btst	-	-	-	-	-	-	-	stby
Class 1													
CMD11	-	-	-	-	data	-	-	-	-	-	-	-	stby
Class 2													
CMD16	-	-	-	-	tran	-	-	-	-	-	-	-	stby
CMD17	-	-	-	-	data	-	-	-	-	-	-	-	stby
CMD18	-	-	-	-	data	-	-	-	-	-	-	-	stby
CMD23	-	-	-	-	tran	-	-	-	-	-	-	-	stby

Table 4-18 : e-NAND State Transition Table

	Current State											
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**btst**	**rcv**	**prg**	**dis**	**ina**	**irq**
Class 3												
CMD20	-	-	-	-	rcv	-	-	-	-	-	-	stby
Class 4												
CMD16	see class 2											
CMD23	see class 2											
CMD24	-	-	-	-	rcv	-	-	-	rcv	-	-	stby
CMD25	-	-	-	-	rcv	-	-	-	rcv	-	-	stby
CMD26	-	-	-	-	rcv	-	-	-	-	-	-	stby
CMD27	-	-	-	-	rcv	-	-	-	-	-	-	stby
Class 6												
CMD28	-	-	-	-	prg	-	-	-	-	-	-	stby
CMD29	-	-	-	-	prg	-	-	-	-	-	-	stby
CMD30	-	-	-	-	data	-	-	-	-	-	-	stby
Class 5												
CMD35	-	-	-	-	tran	-	-	-	-	-	-	stby
CMD36	-	-	-	-	tran	-	-	-	-	-	-	stby
CMD38	-	-	-	-	prg	-	-	-	-	-	-	stby
Class 7												
CMD16	see class 2											
CMD42	-	-	-	-	rcv	-	-	-	-	-	-	stby
Class 8												
CMD55	-	-	-	stby	tran	data	btst	rcv	prg	dis	-	irq
CMD56; RD/WR = 0	-	-	-	-	rcv	-	-	-	-	-	-	stby
CMD56; RD/WR = 1	-	-	-	-	data	-	-	-	-	-	-	stby
Class 9												
CMD39 CMD40	MMCA Optional Command, currently not supported											
Class 10 - 11												
CMD41; CMD43...CMD54, CMD57-CMD59	Reserved											
CMD60...CMD63	Reserved for Manufacturer											

Table 4-19 : Card State Transition Table

4.10 Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit-string corresponding to the response codeword. The code length depends on the response type.
A response always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (card = '0'). A value denoted by 'x' in the tables below indicates a variable entry. All responses except for the type R3 (see below) are protected by a CRC (see Chapter 4.5 for the definition of CRC7). Every command codeword is terminated by the end bit (always '1').

There are five types of responses. Their formats are defined as follows:

R1 (normal response command): code length 48 bit. The bits 45:40 indicate the index of the command to be responded to, this value being interpreted as a binary coded number (between 0 and 63). The status of the e-NAND is coded in 32 bits.
The e-NAND status is described in Chapter 4.11

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	e-NAND status	CRC7	end bit

Table 4-20 : Response R1

● **R1b** is identical to R1 with an optional busy signal transmitted on the data line DAT0. The e-NAND may become busy after receiving these commands based on its state prior to the command reception. Refer to Section for detailed description and timing diagrams.

● **R2** (CID, CSD register): code length 136 bits. The contents of the CID register are sent as a response to the commands CMD2 and CMD10. The contents of the CSD register are sent as a response to CMD9. Only the bits [127...1] of the CID and CSD are transferred, the reserved bit [0] of these registers is replaced by the end bit of the response.

Bit position	47	46	[45:40]	[39:8]	[7:1]
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	check bits	CID or CSD register incl. internal CRC7	end bit

Table 4-21 : Response R2

● **R3** (OCR register): code length 48 bits. The contents of the OCR register is sent as a response to CMD1. The **level coding** is as follows: restricted voltage windows=LOW, card busy=LOW.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	check bits	OCR register	check bits	end bit

Table 4-22 : Response R3

- R4 and R5 : responses are not supported.

4.11 e-NAND Status

The response format R1 contains a 32-bit field named *e-NAND status*. This field is intended to transmit the e-NAND's status information.
Three different attributes are associated with each one of the e-NAND status bits:

- Bit type.

Two types of e-NAND status bits are defined:
(a) **Error bit**. Signals an error condition detected by the e-NAND. These bits are cleared as soon as the response (reporting the error) is sent out.
(b) **Status bit**. These bits serve as information fields only, and do not alter the execution of the command being responded to. These bits are set and cleared in accordance with the e-NAND status.
The Type field of Table 4-23 defines the type of each bit in the e-NAND status register. The symbol E is used to denote an Error bit while the symbol S is used to denote a Status bit.

- Detection mode of Error bits.

Exceptions are detected by the e-NAND either during the command interpretation and validation phase (Response Mode) or during command execution phase (Execution Mode). Response mode exceptions are reported in the response to a STOP_TRANSMISSION command used to terminate the operation or in the response to a GET_STATUS command issued after the operation is completed.
The Det Mode field of Table 4-23 defines the detection mode of each bit in the card status register. The symbol R is used to denote a Response Mode detection while the symbol X is used to denote an Execution Mode detection.
When an error bit is detected in R mode the e-NAND will report the error in the response to the command that raised the exception. The command will not be executed and the associated state transition will not take place. When an error is detected in X mode the execution is terminated. The error will be reported in the response to the next command. The ADDRESS_OUT_OF_RANGE and ADDRESS_MISALIGN exceptions may be detected both in Response and Execution modes. The conditions for each one of the modes are explicitly defined in the Table 4-23.

- Clear Condition:

A - According to the card current state
B - Always related to the previous command. Reception of a valid command will clear it (with a delay of one command)
C - Clear by read.

Bits	Identifier	Type	Det-Mode	Value	Descript	Clear Cond
31	ADDRESS_ OUT_OF_RANGE	E	R	'0'= no error '1'= error	The command's address argument was out of the allowed range for this e-NAND.	C
			X		A multiple block or stream read/write operation is (although started in a valid address) attempting to read or write beyond the e-NAND capacity	
30	ADDRESS_MISALIGN	E	R	'0'= no error '1'= error	The command' s address argument (in accordance with the currently set block length) positions the first data block misaligned to the e-NAND physical blocks.	C
			X		A multiple block read/write operation (although started with a valid address/block-length combination) is attempting to read or write a data block which does not align with the physical blocks of the e-NAND.	
29	BLOCK_LEN_ERROR	E	R	'0'= no error '1'= error	Either the argument of a SET_BLOCKLEN command exceeds the maximum value allowed for the e-NAND, or the previously defined block length is illegal for the current command (e.g. the host issues a write command, the current block length is smaller than the e-NAND's maximum and write partial blocks is not allowed)	C
28	ERASE_SEQ_ERROR	E	R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E	X	'0'= no error '1'= error	An invalid selection of erase groups for erase occurred.	C
26	WP_VIOLATION	E	X	'0'= no error '1'= error	Attempt to program a write protected block.	C
25	CARD_IS_LOCKED	S	R	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A
24	LOCK_UNLOCK_ FAILED	E	X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command	C
23	COM_CRC_ERROR	E	R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E	R	'0'= no error '1'= error	Command not legal for the e-NAND state	B
21	CARD_ECC_FAILED	E	X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E	R	'0'= no error '1'= error	(Undefined by the standard) A card error occurred, which is not related to the host command.	C

Table 4-23 : e-NAND Status

Bits	Identifier	Type	Det-Mode	Value	Descript	Clear Cond
19	ERROR	E	X	'0'= no error '1'= error	(Undefined by the standard) A generic e-NAND error related to the (and detected during) execution of the last host command (e.g. read or write failures).	C
18 - 17	Not applicable. This bit is always set to 0.					
16	CID/ CSD_OVERWRITE	E	X	'0'= no error '1'= error	Can be either one of the following errors: - The CID register has been already written and can not be overwritten - The read only section of the CSD does not match the e-NAND content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
15	WP_ERASE_SKIP	E	X	'0'= not protected '1'= protected	Only partial address space was erased due to existing write protected blocks.	C
14	Reserved, must be set to 0					
13	ERASE_RESET	E	R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received (commands other than CMD35, CMD36, CMD38 or CMD13	C
12:9	CURRENT_STATE	S	R	0 = Idle 1 = Ready 2 = Ident 3 = Stby 4 = Tran 5 = Data 6 = Rcv 7 = Prg 8 = Dis 9 = Btst 10 =slp 11-15 = reserved	The state of the e-NAND when receiving the command. If the command execution causes a state change, it will be visible to the host in the response on the next command. The four bits are interpreted as a binary number between 0 and 15.	B
8	READY_FOR_DATA	S	R	'0'= not ready '1'= ready	Corresponds to buffer empty signalling on the bus	A
7	SWITCH_ERROR	E	X	'0'= no error '1'= switch error	If set, the e-NAND did not switch to the expected mode as requested by the SWITCH command	C
6	Reserved					
5	Not applicable. This bit is always set to 0.					
4	Reserved					
3:2	Reserved for Application Specific commands					
1:0	Reserved for Manufacturer Test Mode					

Table 4-24 : e-NAND Status

4.12 Memory Array Partitioning

The basic unit of data transfer to/from the e-NAND is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity. For block oriented commands, the following definition is used:

- **Block**: is the unit which is related to the block oriented read and write commands. Its size is the number of bytes which will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.

For R/W e-NANDs, special erase and write protect commands are defined:

The granularity of the erasable units is the **Erase Group:** The smallest number of consecutive write blocks which can be addressed for erase. The size of the Erase Group is e-NAND specific and stored in the CSD when ERASE_GROUP_DEF is enabled.
The granularity of the Write Protected units is the **WP-Group:** The minimal unit which may be individually write protected.
Its size is defined in units of erase groups. The size of a WP-group is e-NAND specific and stored in the CSD when ERASE_GROUP_DEF is disabled, and in the EXT_CSD when ERASE_GROUP_DEF is enabled.

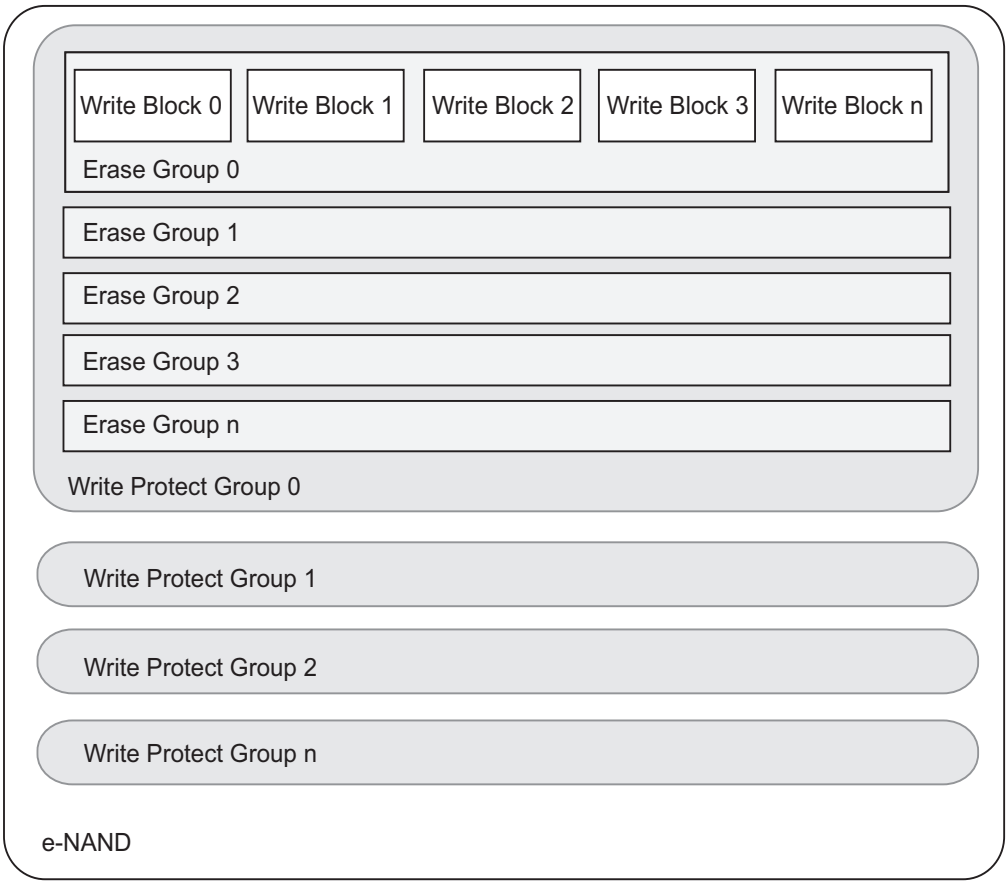


Figure 4-9 : Memory Array Partitioning

4.13 Timing Diagrams

All timing diagrams use the following schematics and abbreviations:

Symbol	Definition
S	Start bit (= '0')
T	Transmitter bit (Host = '1', e-NAND = '0')
P	One-cycle pull-up (= '1')
E	End bit (='1')
L	One-cycle pull-down (= '0')
Z	High impedance state (-> = '1')
X	Driven value, '1' or '0'
D	Data bits
*	Repetition
CRC	Cyclic redundancy check bits (7 bits)
	e-NAND active
	Host active

Table 4-25 : Timing Diagram Symbols

The difference between the P-bit and Z-bit is that a P-bit is actively driven to HIGH by the e-NAND respectively host output driver, while Z-bit is driven to (respectively kept) HIGH by the pull-up resistors RCMD respectively RDAT. Actively-driven Pbits are less sensitive to noise.
All timing values are defined in Table 4-25.

4.13.1 Command and Response

Both host command and e-NAND response are clocked out with the rising edge of the host clock.

- **e-NAND identification and e-NAND operation conditions timing**

The card (e-NAND) identification (CMD2) and card (e-NAND) operation conditions (CMD1) timing are processed in the open-drain mode. The e-NAND response to the host command starts after exactly NID clock cycles.

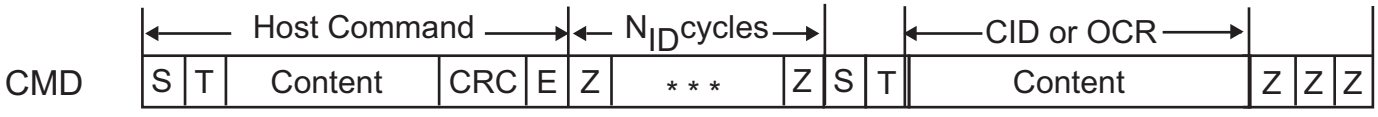


Figure 4-10 : Identification Timing (e-NAND Identification Mode)

● **Assign a e-NAND relative address**

The SET_RCA (CMD 3) is also processed in the open-drain mode. The minimum delay between the host command and e-NAND response is NCR clock cycles.

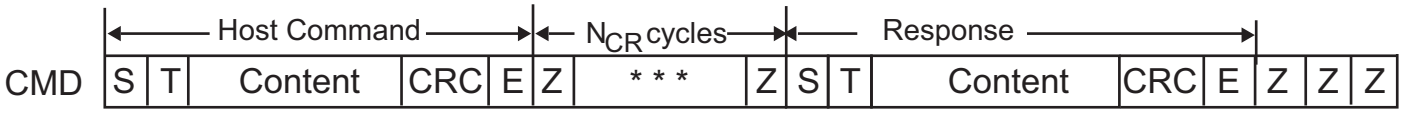


Figure 4-11 : SET_RCA Timing (e-NAND Identification Mode)

● **Data transfer mode.**

After a e-NAND receives its RCA it will switch to data transfer mode. In this mode the CMD line is driven with push-pull drivers.

The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and than by P bits pushed up by the responding e-NAND. This timing diagram is relevant for all responded host commands except CMD1,2,3:

Figure 4-12 : Command Response Timing (Data Transfer Mode)

● **R1b Responses**

Some commands, like CMD6, may assert the BUSY signal after responding with R1. If the busy signal is asserted, it is done two clock cycles after the end bit of the command. the DAT0 line is driven low, DAT1-DAT7 lines are driven by the e-NAND though their value is not relevant.

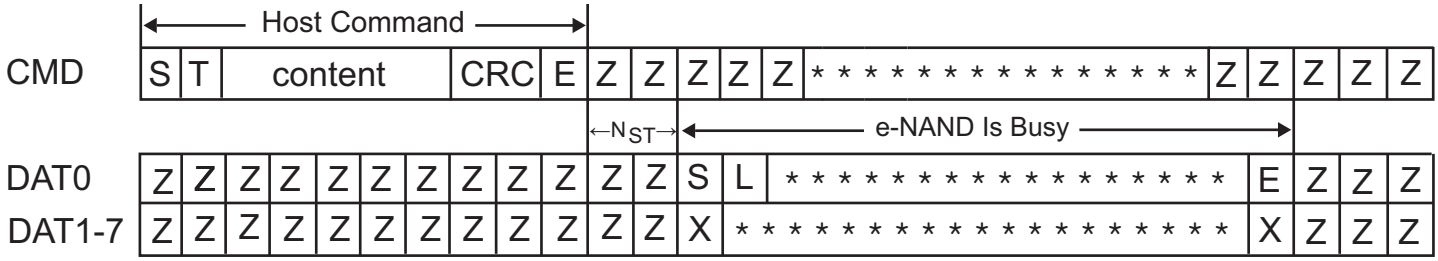


Figure 4-13 : R1b Response Timing

● **Last e-NAND Response - Next Host Command Timing**

After receiving the last e-NAND response, the host can start the next command transmission after at least NRC clock cycles. This timing is relevant for any host command.

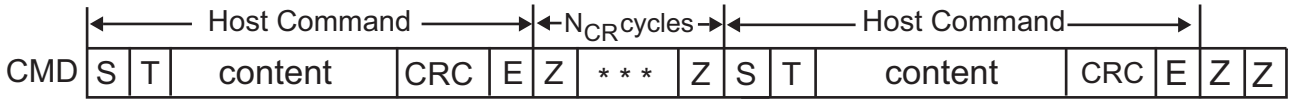


Figure 4-14 : Timing Response End To Next Command Start (Data Transfer Mode)

Last Host Command - Next Host Command Timing

After the last command has been sent, the host can continue sending the next command after at least NCC clock periods.

If the ALL_SEND_CID command is not responded by the e-NAND after NID + 1 clock periods, the host can conclude there is no e-NAND present in the bus.

Figure 4-15 : Timing Of Command Sequences (All Modes)

4.14 Data Read

● **Single Block Read**

The host selects one e-NAND for data read operation by CMD7, and sets the valid block length for block oriented data transfer by CMD16. The basic bus timing for a read operation is given in Figure 4-16. The sequence starts with a single block read command (CMD17) which specifies the start address in the argument field. The response is sent on the CMD line as usual.

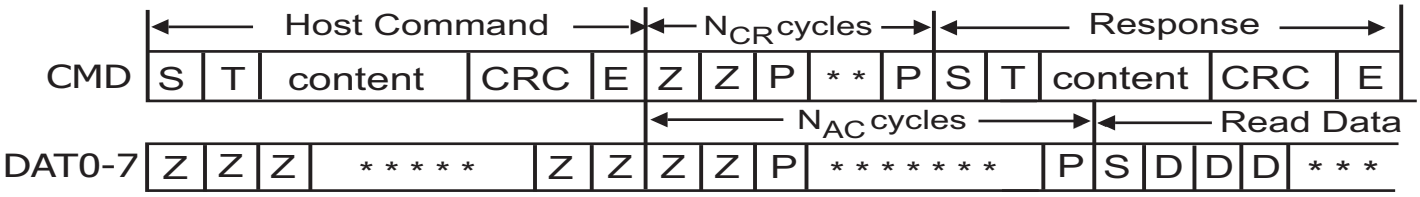


Figure 4-16 : Single Block Read Timing

Data transmission from the e-NAND starts after the access time delay NAC beginning from the end bit of the read command.

After the last data bit, the CRC check bits are suffixed to allow the host to check for transmission errors.

● **Multiple Block Read**

In multiple block read mode, the e-NAND sends a continuous flow of data blocks following the initial host read command. The data flow is terminated by a stop transmission command (CMD12). Figure 4-17 describes the timing of the data blocks and Figure 4-18 the response to a stop command. The data transmission stops two clock cycles after the end bit of the stop command.

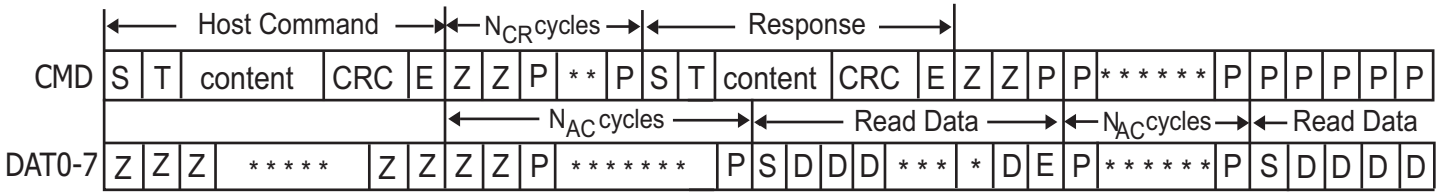


Figure 4-17 : Multiple Block Read Timing

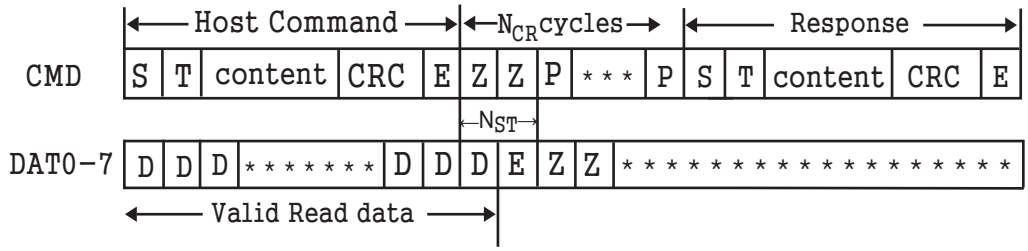


Figure 4-18 : Stop Command Timing (CMD12, Data Transfer Mode)

4.15 Data Write

● **Single Block Write**

The host selects the e-NAND for data write operation by CMD7.

The host sets the valid block length for block oriented data transfer (a stream write mode is also available) by CMD16.

The basic bus timing for a write operation is given in Figure 4-19. The sequence starts with a single block write command (CMD24) which determines (in the argument field) the start address. It is responded by the e-NAND on the CMD line as usual.

The data transfer from the host starts NWR clock cycles after the e-NAND response was received.

The data is suffixed with CRC check bits to allow the e-NAND to check it for transmission errors. The e-NAND sends back the CRC check result as a CRC status token on DAT0. In the case of transmission error, occurring on any of the active data lines, the e-NAND sends a negative CRC status (101) on DAT0. In the case of successful transmission, over all active data lines, the e-NAND sends a positive CRC status (010) on DAT0 and starts the data programming procedure

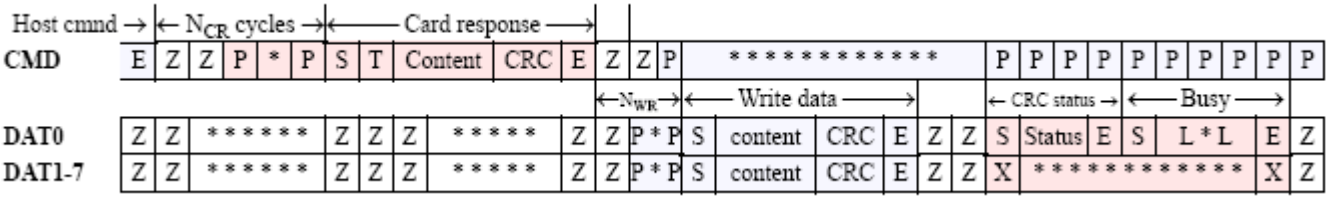


Figure 4-19 : Block Write Command Timing

While the card is programming it indicates busy by pulling down the Dat0 line. This busy status is directly related to Programming state. As soon as the card completes the programming it stops pulling down the Dat0 line.

● **Multiple Block Write**

In multiple block write mode, the e-NAND expects continuous flow of data blocks following the initial host write command. The data flow is terminated by a stop transmission command (CMD12). Figure 4-20 describes the timing of the data blocks with and without e-NAND busy signal.

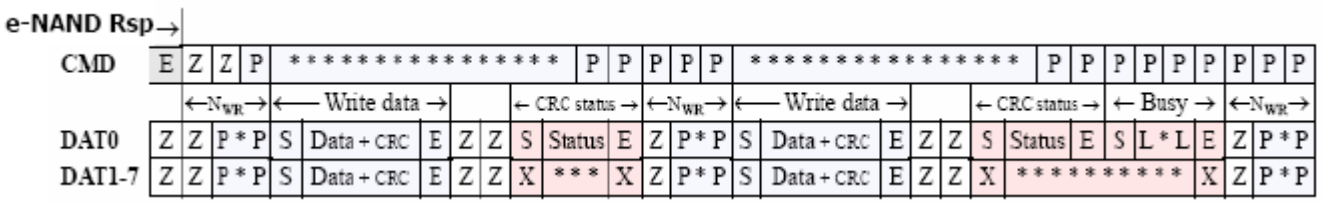


Figure 4-20 : Multiple Block Write Timing

The stop transmission command works similar as in the read mode. Figure 4-21 to Figure 4-24 describe the timing of the stop command in different e-NAND states.

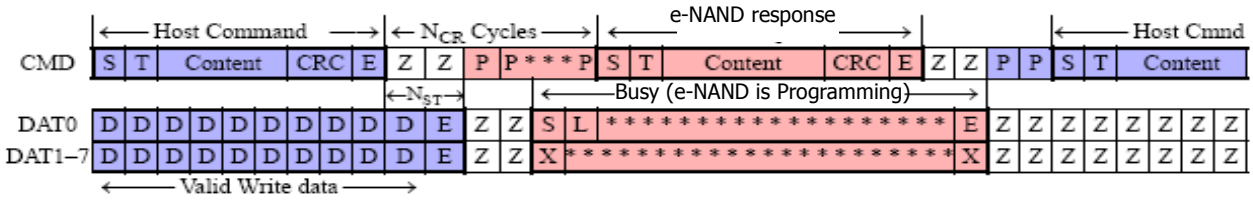
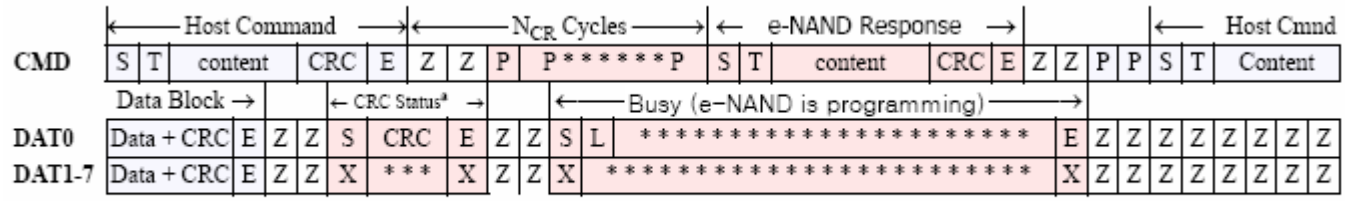


Figure 4-21 : Stop Transmission During Data Transfer From The Host

The e-NAND will treat a data block as successfully received and ready for programming only if the CRC data of the block was validated and the CRC status tokens sent back to the host. Figure 4-21 is an example of an interrupted (by a host stop command) attempt to transmit the CRC status block. The sequence is identical to all other stop transmission examples. The end bit of the host command is followed, on the data lines, with one more data bit, an end bit and two Z clocks for switching the bus direction. The received data block, in this case is considered incomplete and will not be programmed.



a.The card CRC status response is interrupted by the host.

Figure 4-22 : Stop Transmission During CRC Status Transfer From The e-NAND

All previous examples dealt with the scenario of the host stopping the data transmission during an active data transfer. The following two diagrams describe a scenario of receiving the stop transmission between data blocks. In the first example the e-NAND is busy programming the last block while in the second the e-NAND is idle. However, there are still unprogrammed data blocks in the input buffers. These blocks are being programmed as soon as the stop transmission command is received and the e-NAND activates the busy signal.

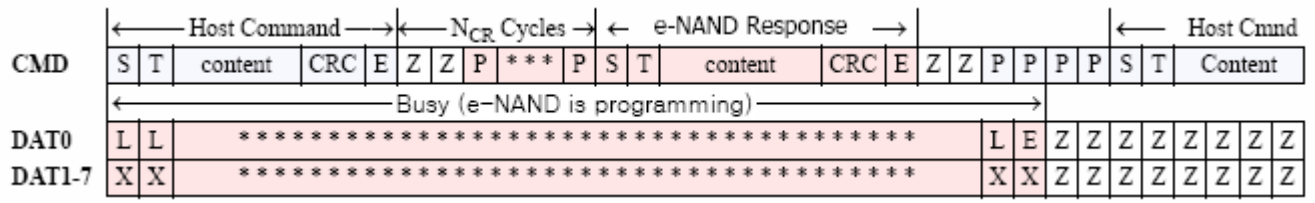


Figure 4-23 : Stop Transmission After Last Data Block. e-NAND Is Busy Programming.

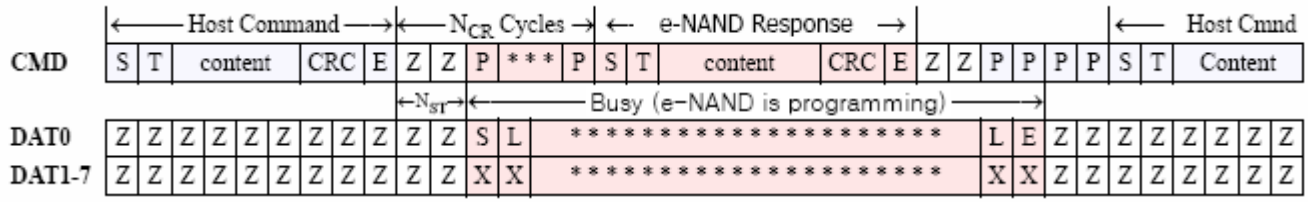


Figure 4-24 : Stop Transmission After Last Data Block. e-NAND Becomes Busy.

- **Erase, Set and Clear Write Protect Timing**

The host must first select the erase groups to be erased using the erase start and end command (CMD35, CMD36). The erase command (CMD38), once issued, will erase all selected erase groups. Similarly, set and clear write protect commands start a programming operation as well. The e-NAND will signal busy (by pulling the DAT0 line low) for the duration of the erase or programming operation. The bus transaction timings are identical to the variation of the stop transmission described in Figure 4-24.

- **Reselecting a busy e-NAND**

When a busy e-NAND which is currently in the dis state is reselected it will reinstate its busy signaling on the data line DAT0.
The timing diagram for this command / response / busy transaction is given in Figure 4-24.

4.16 Bus Test Procedure Timing

After reaching the Tran-state a host can initiate the Bus Testing procedure. If there is no response to the CMD19 sent by the host, the host should read the status from the e-NAND with CMD13. If there was no response to CMD19, the host may assume that this function is not supported by the e-NAND.

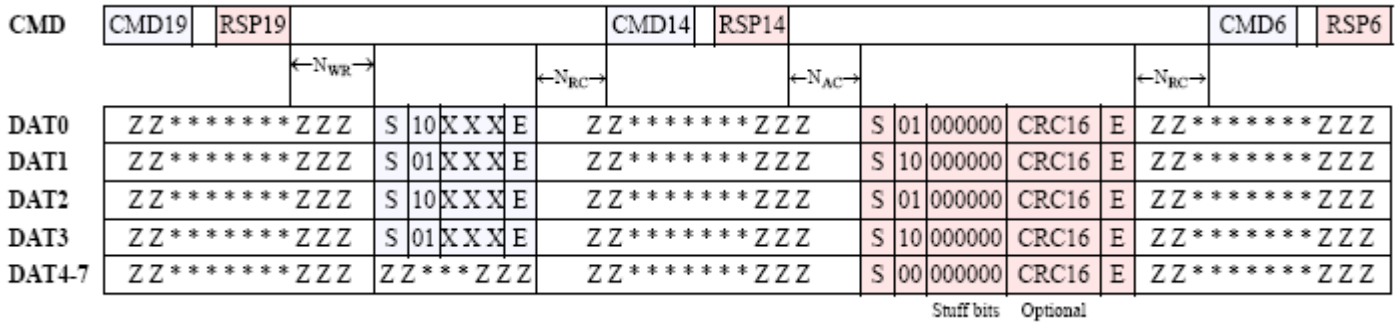


Figure 4-25 : 4 bit System Bus Testing Procedure

4.17 Boot operation

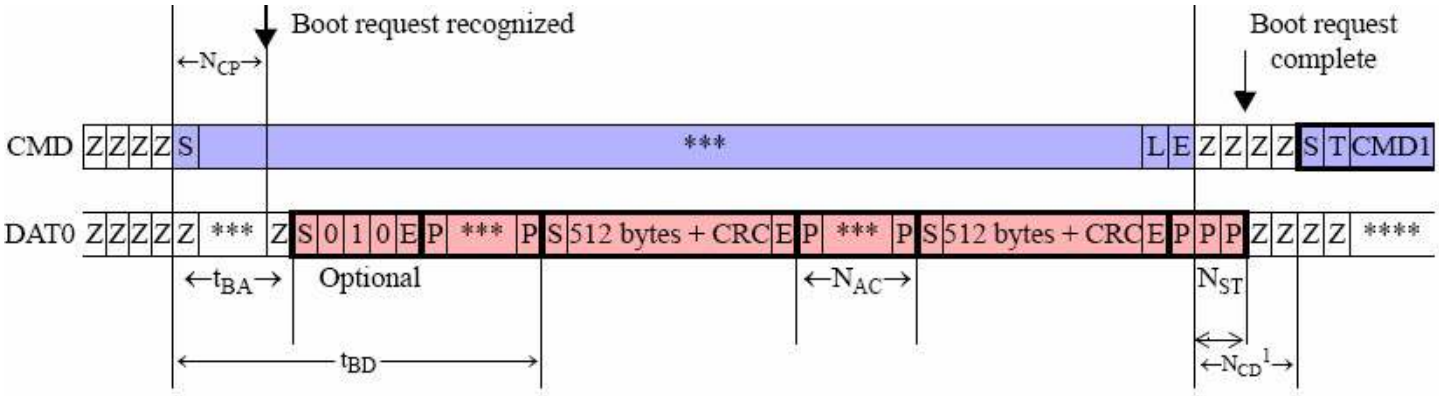


Figure 4-26: Boot operation, termination between consecutive data blocks

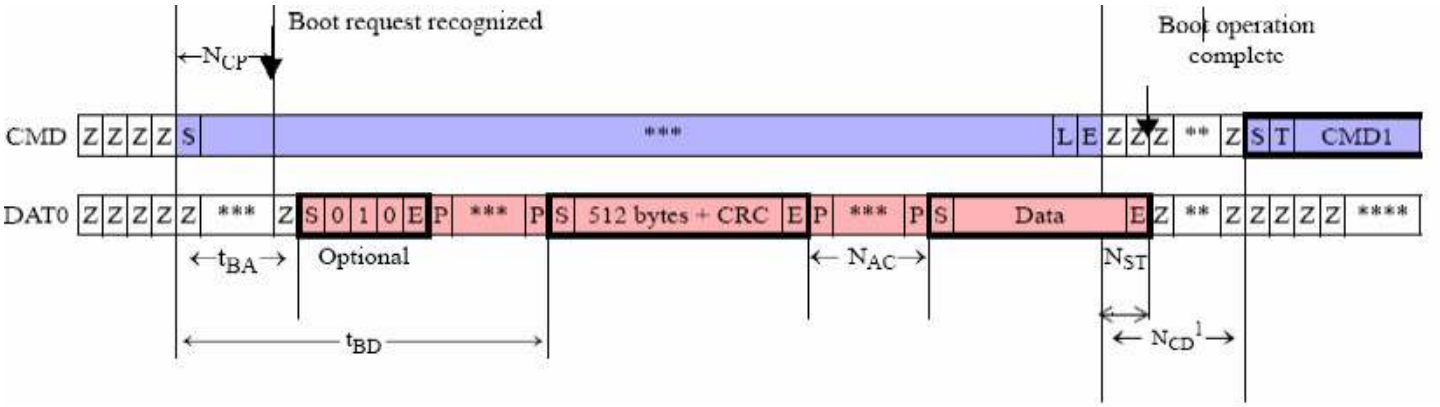


Figure 4-27: Boot operation, termination during transfer

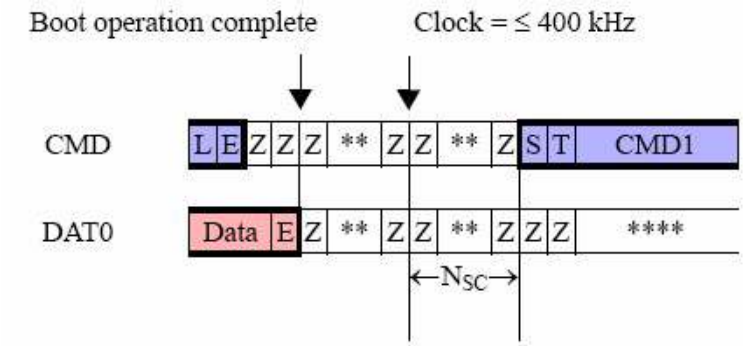
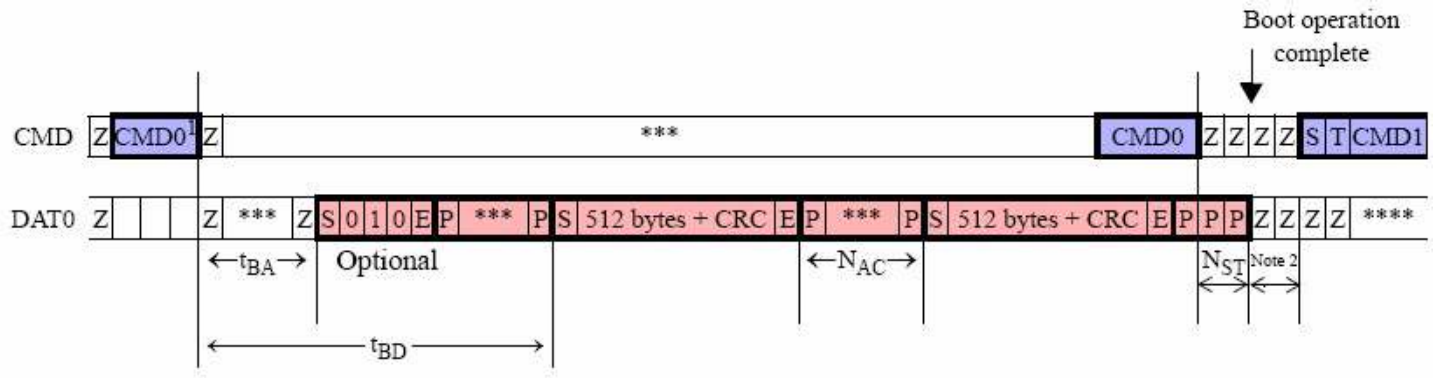


Figure 4-28: Bus mode change timing (push-pull to open drain)

4.17.1 Alternative Boot operation (device optional)



NOTE 1. CMD0 with argument 0xFFFFFFFA.

NOTE 2. Refer to Figure 4-28

Figure 4-29: Alternative boot operation, termination between consecutive data blocks

4.18 Timing Values

Symbol	Min	Max	Unit
N_{AC}	2	10 * (TAAC *F_{OP} + 100 * NSAC)[a]	clock cycles
N_{CC}	8	-	clock cycles
N_{CD}	56	-	clock cycles
N_{CP}	74	-	clock cycles
N_{CR}	2	64	clock cycles
N_{ID}	5	5	clock cycles
N_{RC}	8	-	clock cycles
N_{SC}	8	-	clock cycles
N_{ST}	2	2	clock cycles
N_{WR}	2	-	clock cycles
BA	-	50	ms
BD	-	1	s

a. F_{OP} is the e-NAND clock frequency the host is using for the read operation.

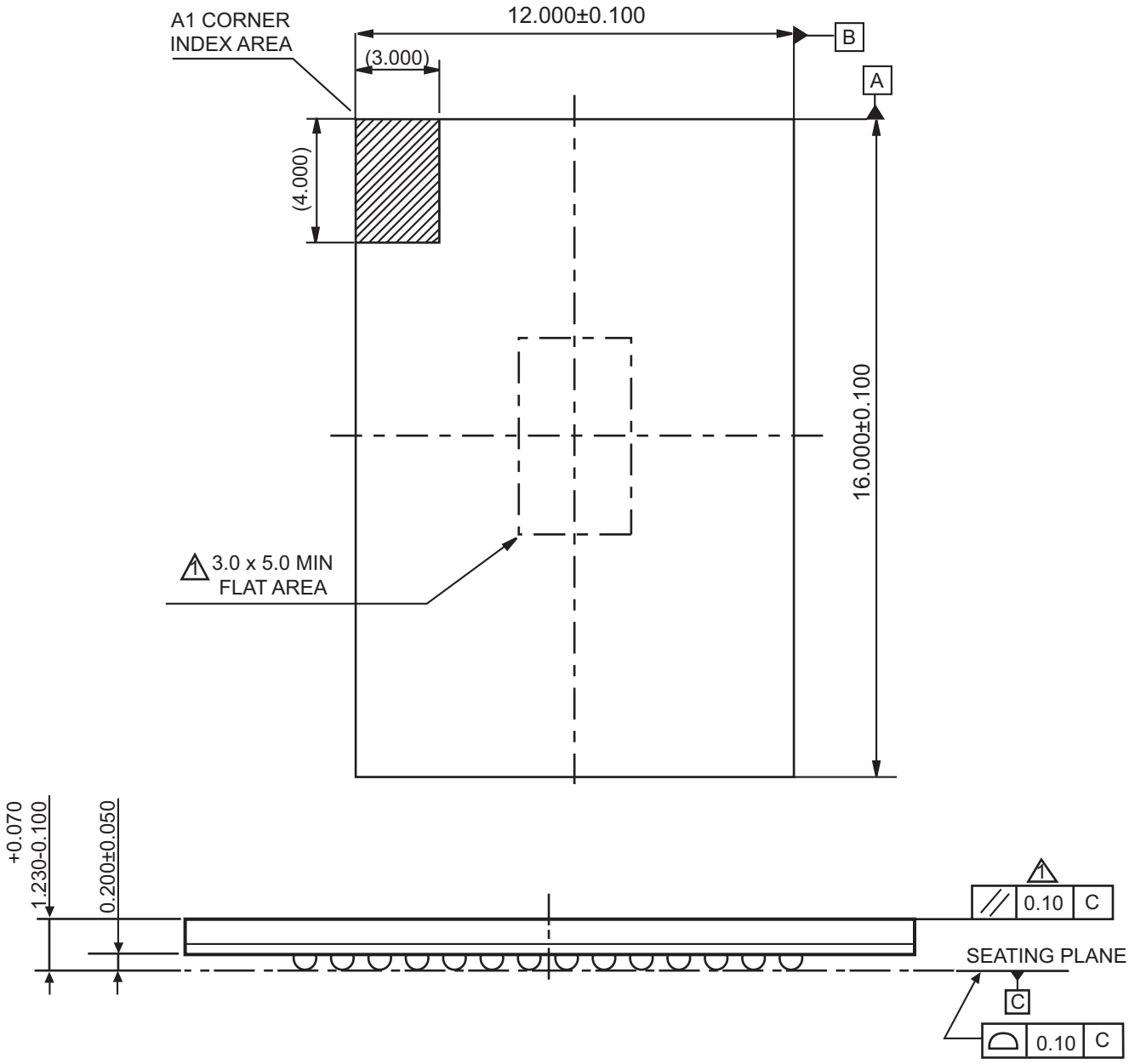
Following is a calculation example:

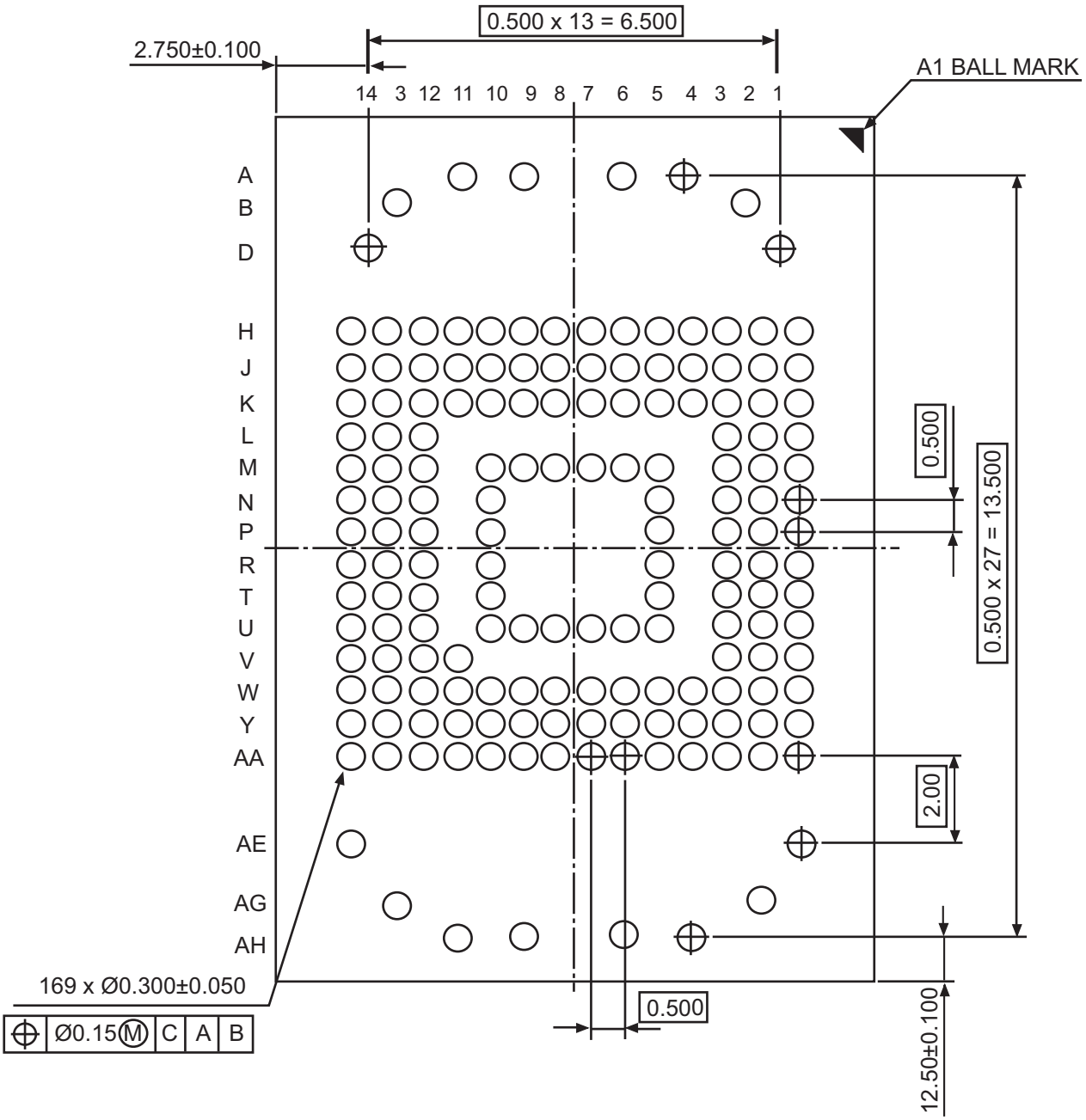
CSD value for TAAC is 0x26; this is equal to 1.5mSec;

CSD value for NSAC is 0;
The host frequency F_{OP} is 10MHz

N_{AC} = 10 x ($1.5 \times 10^{-3} \times 10 \times 10^{6}$ + 0) = 150,000 clock cycles

PKG Mechnical Drowing




0.500 x 13 = 6.500
2.750±0.100
A1 BALL MARK
14 3 12 11 10 9 8 7 6 5 4 3 2 1
A
B
D
H
J
K
L
M
N
P
R
T
U
V
W
Y
AA
AE
AG
AH
0.500
0.500 x 27 = 13.500
2.00
169 x Ø0.300±0.050
Ø0.15Ⓜ C A B
0.500
12.50±0.100